EE 505

Lecture 8

Duty Cycle Effects
Clock Jitter
Statistical Circuit Modeling

Review from last lecture

Windowing - a strategy to address the problem of requiring precisely an integral number of periods to use the DFT for Spectral analysis?

- Windowing is sometimes used
- Windowing is sometimes misused

Review from last lecture

Windowing

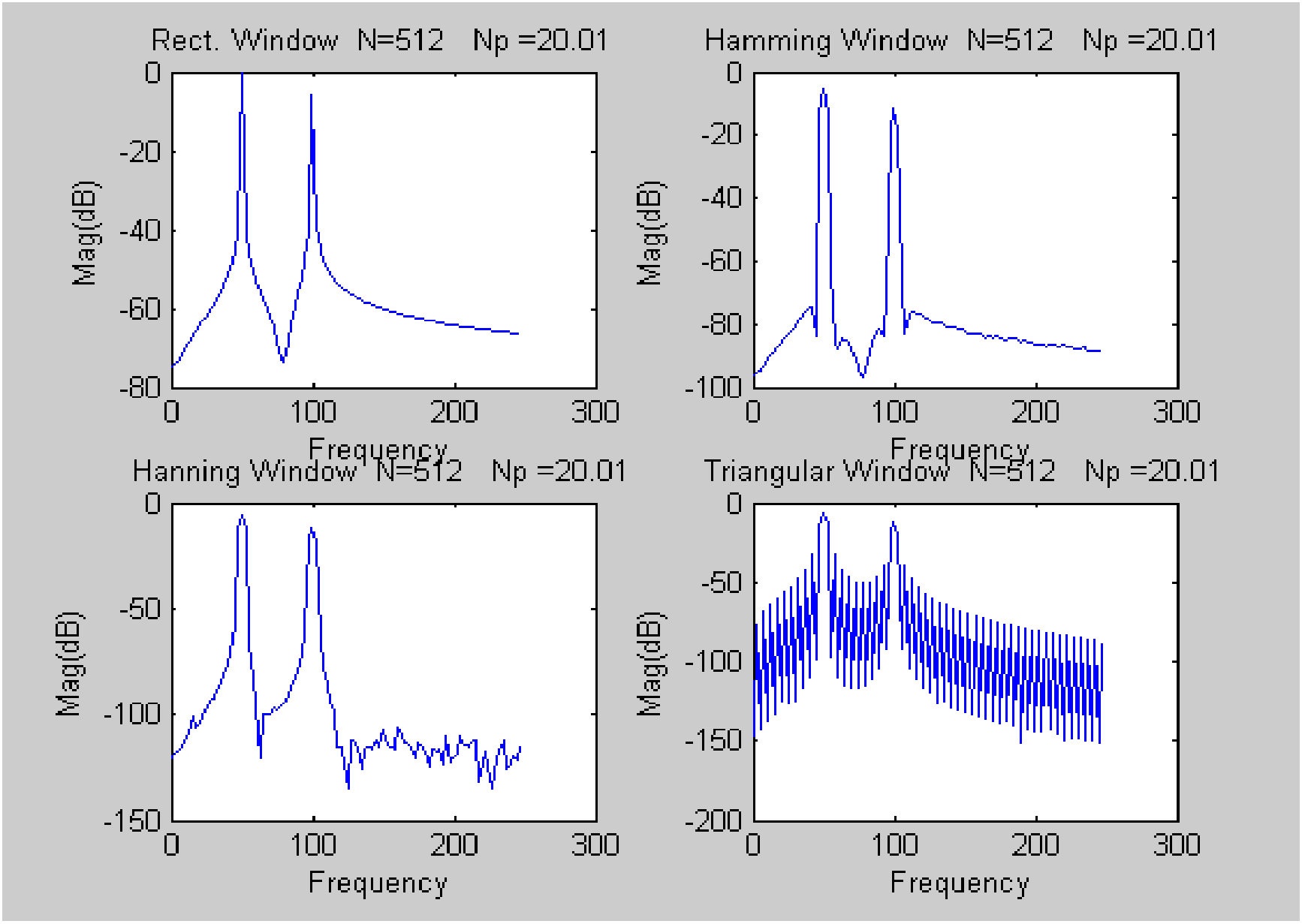
Windowing is the weighting of the time domain function to maintain continuity at the end points of the sample window

Well-studied window functions:

- Rectangular (also with appended zeros)
- Triangular
- Hamming
- Hanning
- Blackman

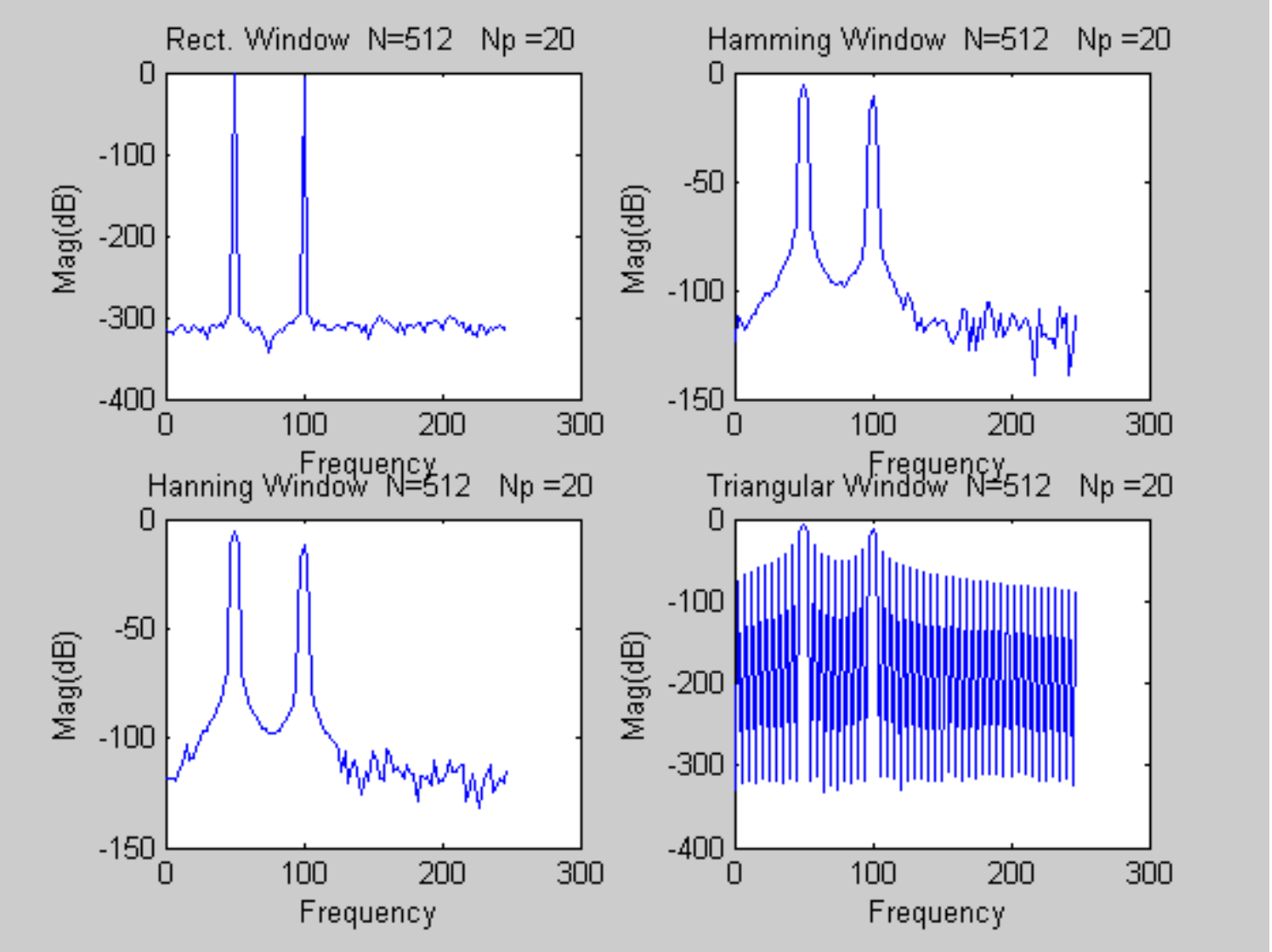
Review from last lecture

Comparison of 4 windows



Review from last lecture

Comparison of 4 windows



Review from last lecture

Preliminary Observations about Windows

- Provide separation of spectral components
- Energy can be accumulated around spectral components
- Simple to apply
- Some windows work much better than others

But – windows do not provide dramatic improvement and can significantly degrade performance if sampling hypothesis are met

Review from last lecture

Quantization Effects

time and amplitude depicted

Zero-order sample/hold on DAC or zero-order hold on ADC interpreted output

DAC

Assume DAC will be used to generate a continuous time signal

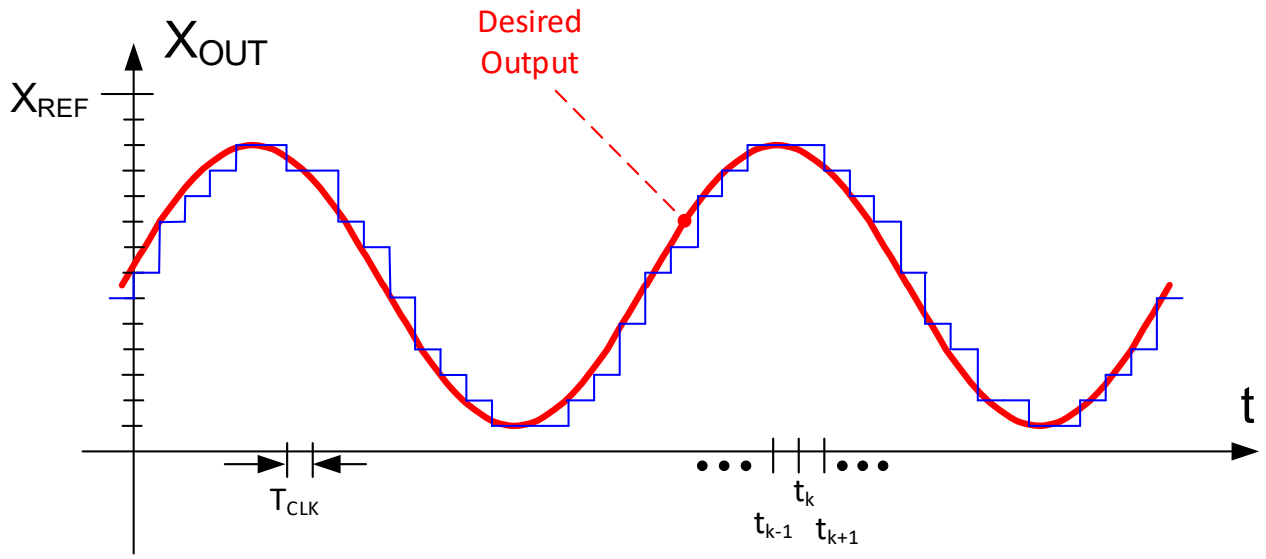
Assume DAC is driven by a clock of period T_{CLK}

DAC inputs will be a discrete sequence $\vec{X}(t_k) = \langle x_{quant}(t_k) \rangle$

DAC inputs can change only at times t_k

The duration of each DAC input depends upon system

With zero-order S/H, it is assumed that the DAC output remains constant between transaction times $x_{OUT}(t) = x_{quant}(t_k) \qquad t_k \le t < t_{k+1}$

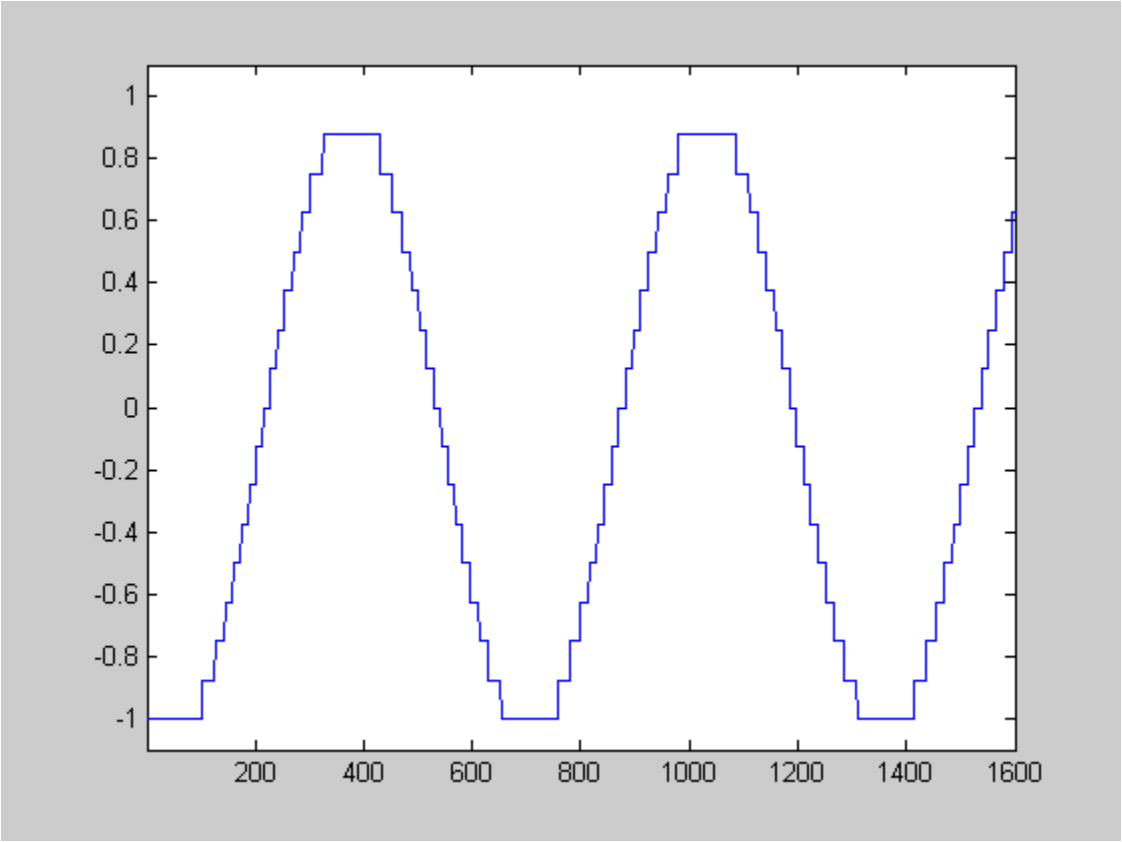


Review from last lecture

Quantization Effects

(time and amplitude depicted)

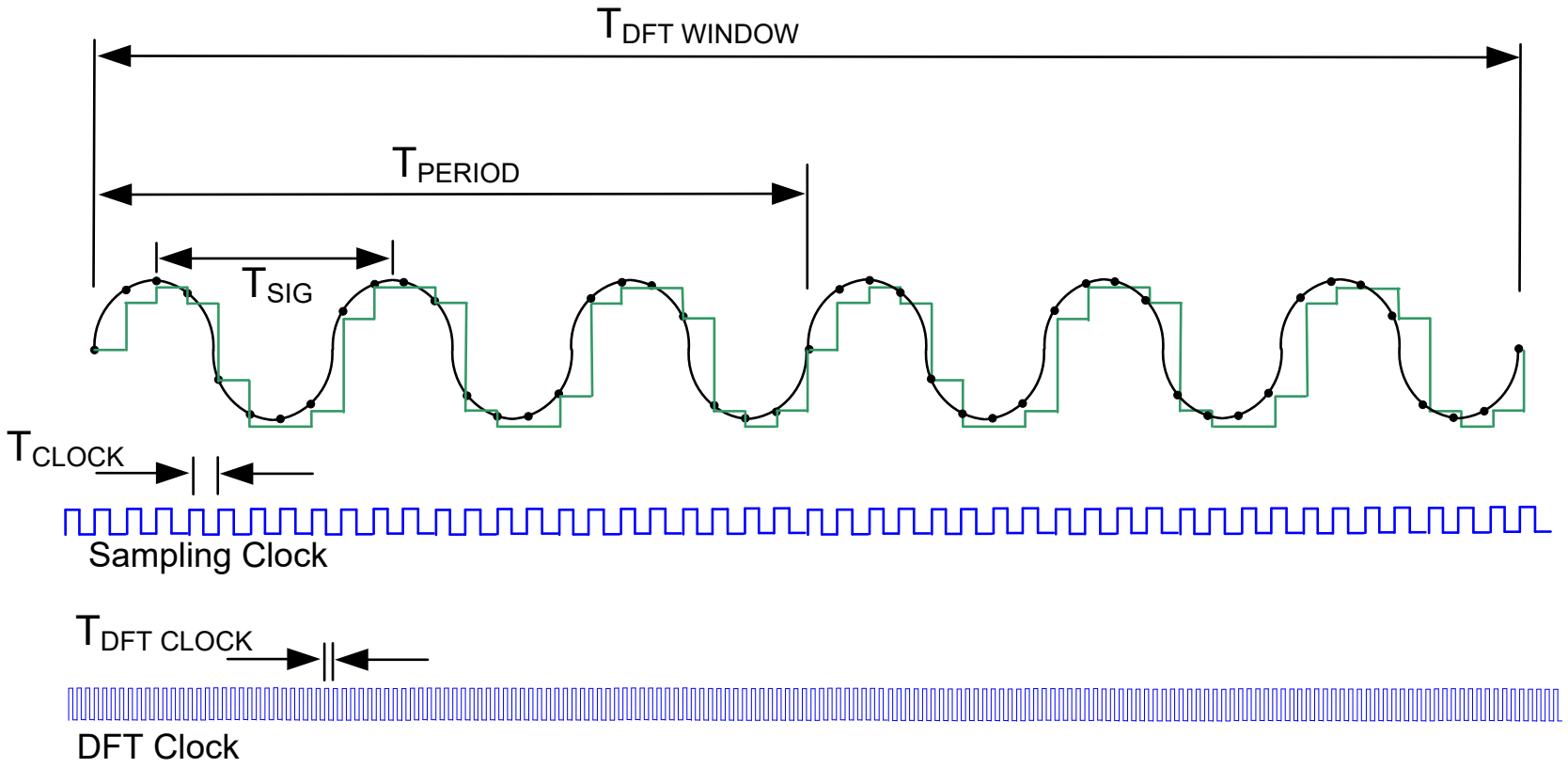
16,384 pts res = 4bits



Is this signal band limited?

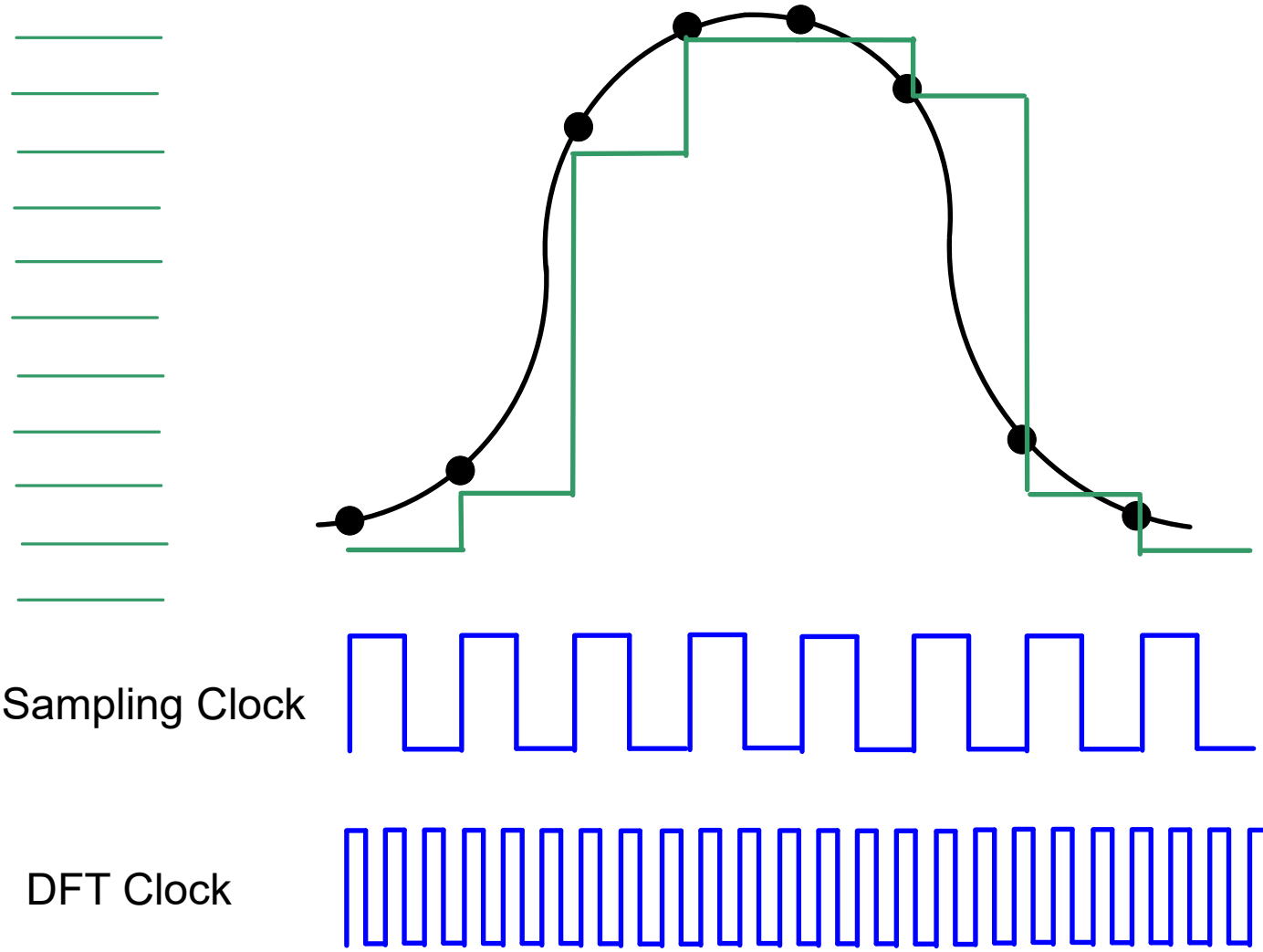
Review from last lecture

Spectral Characteristics of DAC



Review from last lecture

Spectral Characteristics of DAC



Review from last lecture

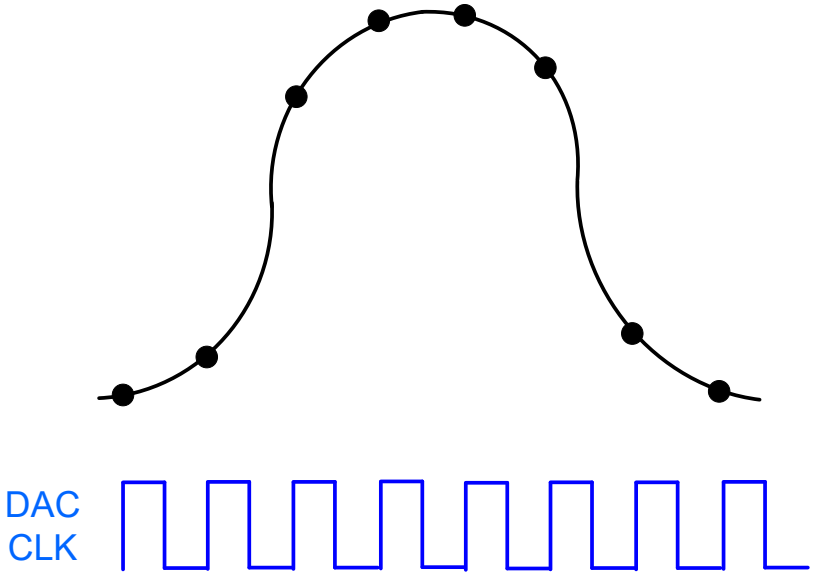
Summary of time and amplitude quantization assessment

Time and amplitude quantization do not introduce harmonic distortion

Time and amplitude quantization do increase the noise floor

Duty Cycle Effects on Spectral Performance of DACS

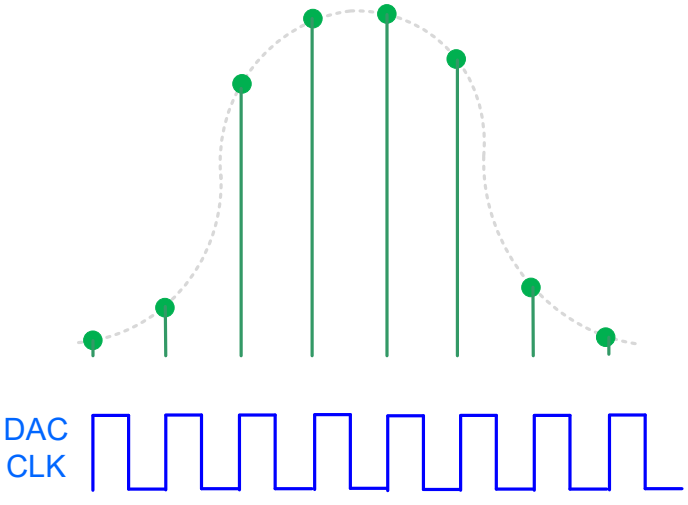
(File: DAC Quantization with RTZ.m)



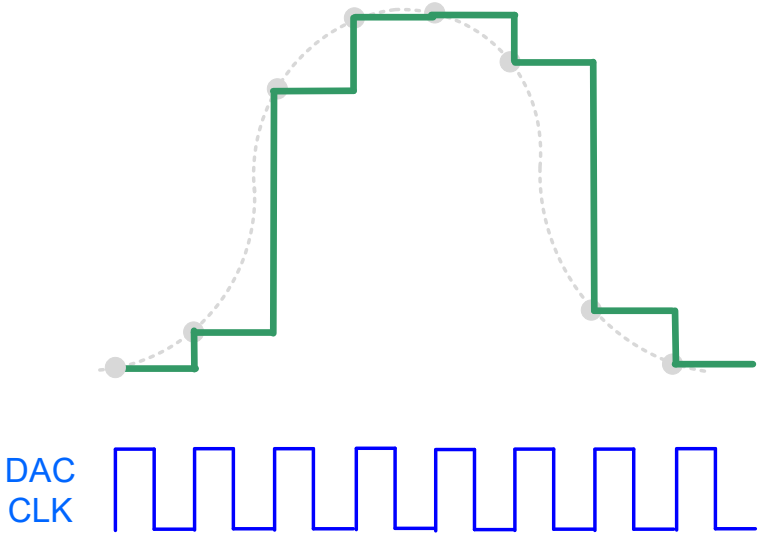
What type of DAC output is desired?

Duty Cycle Effects on Spectral Performance of DACS

(File: DAC Quantization with RTZ.m)



Impulse Output

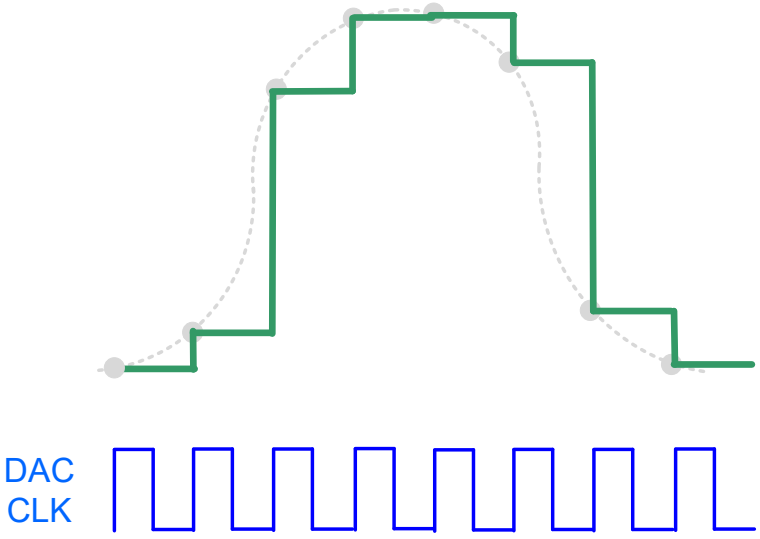


Zero-order Sample and Hold

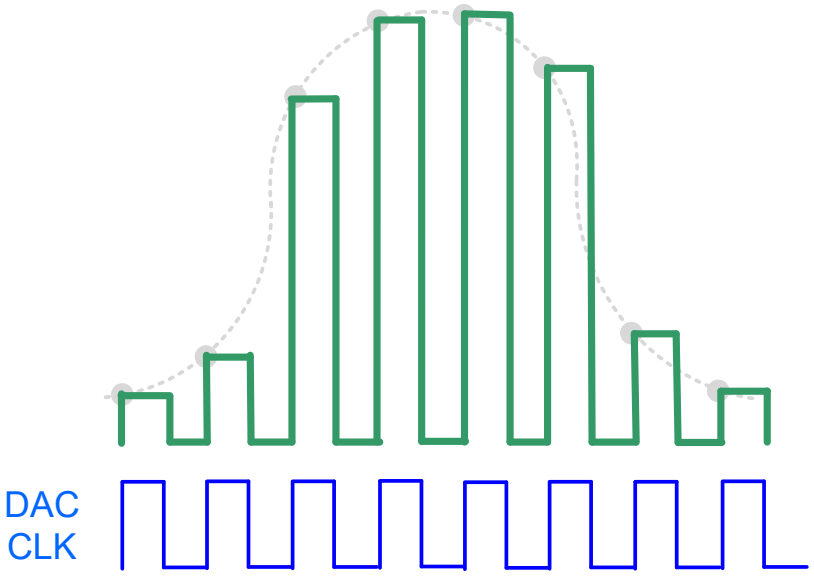
(100% duty cycle)

Duty Cycle Effects on Spectral Performance of DACS

(File: DAC Quantization with RTZ.m)



Zero-order Sample and Hold
(100% duty cycle)



Zero-order Sample and Hold
(50% duty cycle)

Return to Zero

Consider

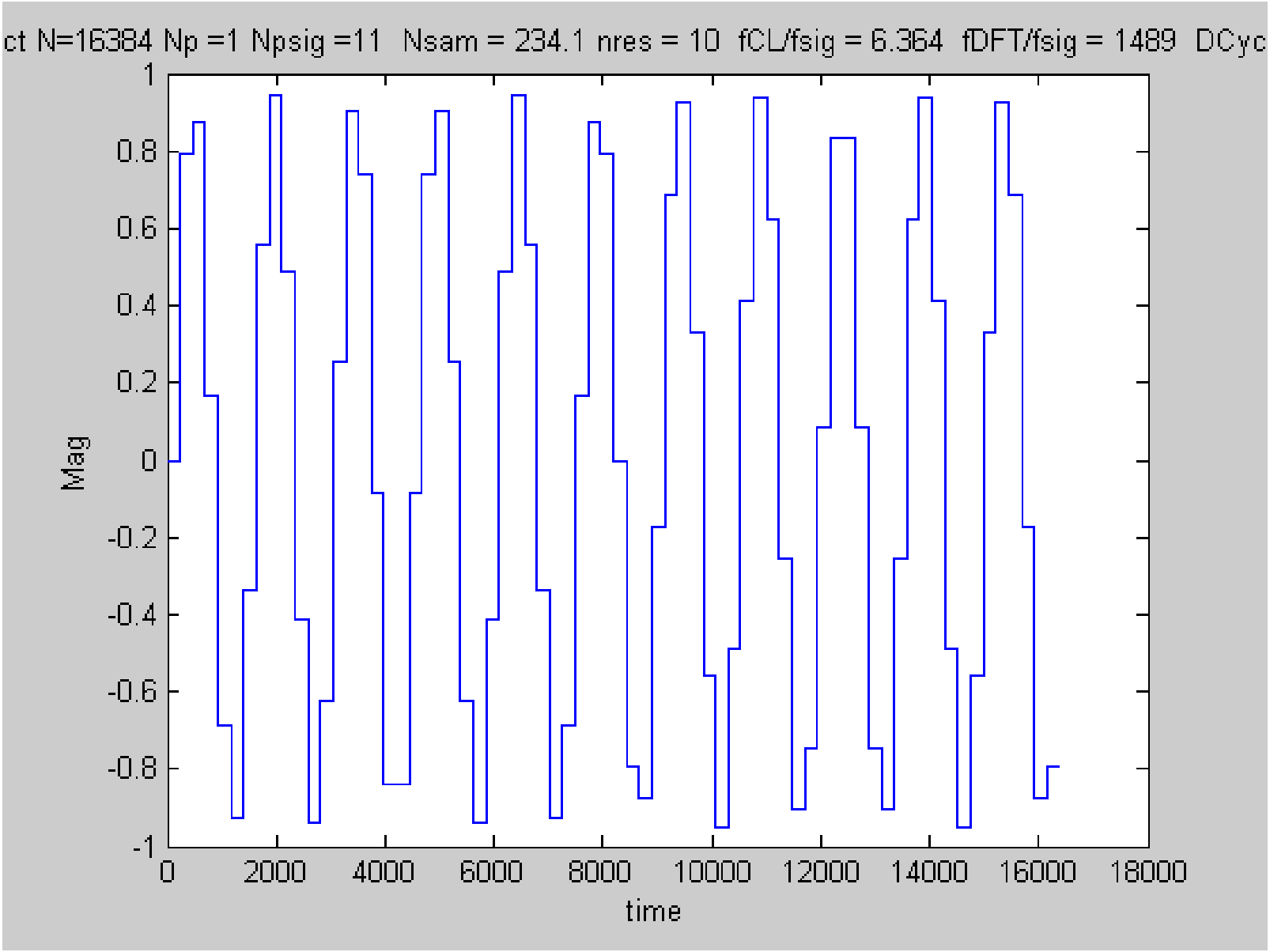
$N_P=1$
$N_{SIG}=11$
$N_{CL}=70$
$f_{sig}=50$
$n_{res}=10$

Thus, $f_{CLK}=f_{SIG}(N_{CL}/N_{SIG})=318Hz$

The fft spectrum should be nominally symmetric around $f_{CLK}/2=159Hz$ so will get only the fundamental, second harmonic, and third harmonic in the fundamental frequency half-period which occurs at fft coefficient number 36 and the clock frequency will be at fft coefficient number 71 (and thus the fundamental will appear at fft coefficient numbers 11+1=12 and 71-11=60)

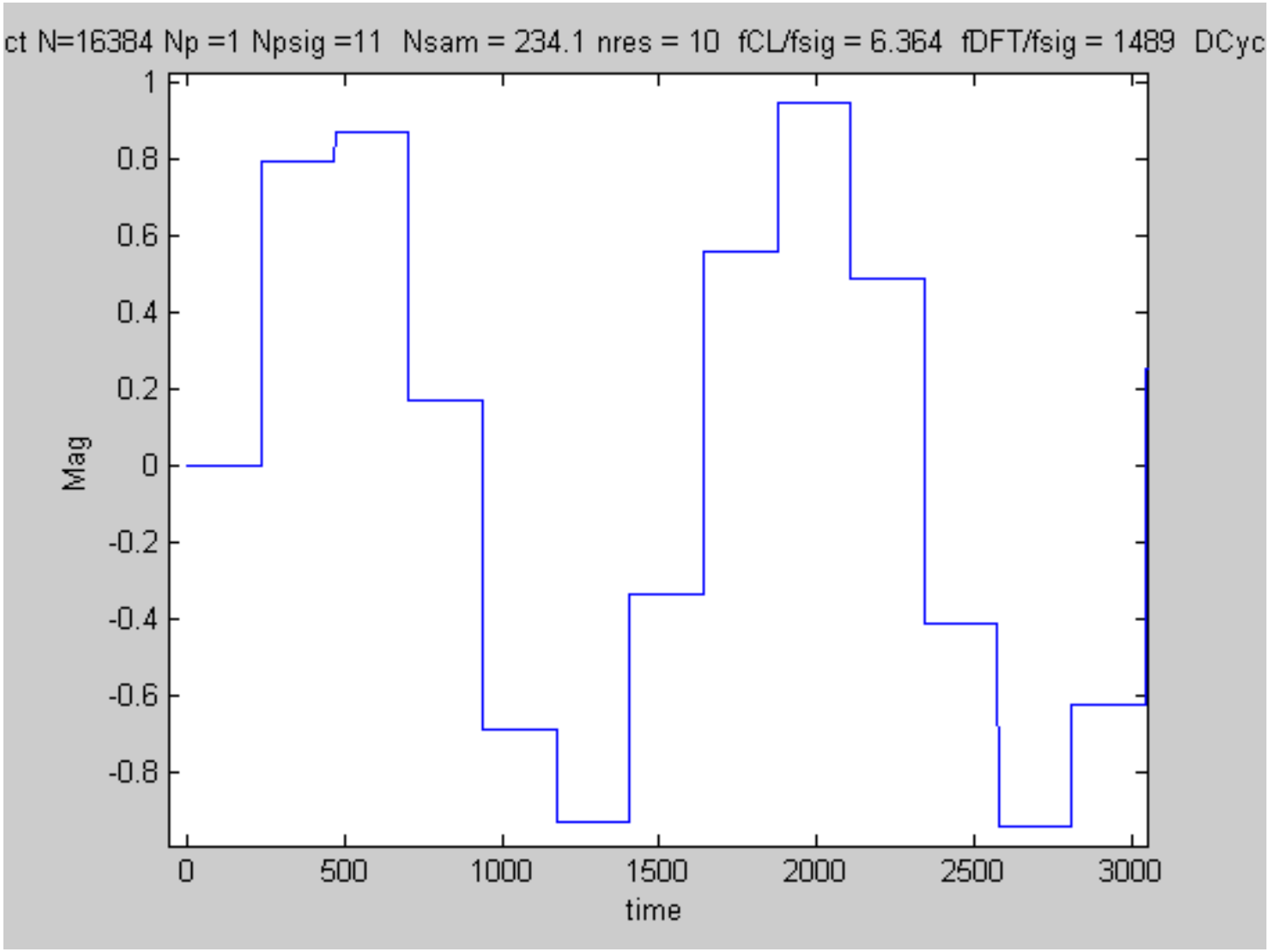
The relationship between fft coefficient number and frequency is given by

$$f=\left(\frac{n-1}{N_{SIG}}\right)f_{SIG} \quad \text{or by} \quad n=1+f\left(\frac{N_{SIG}}{f_{SIG}}\right)$$

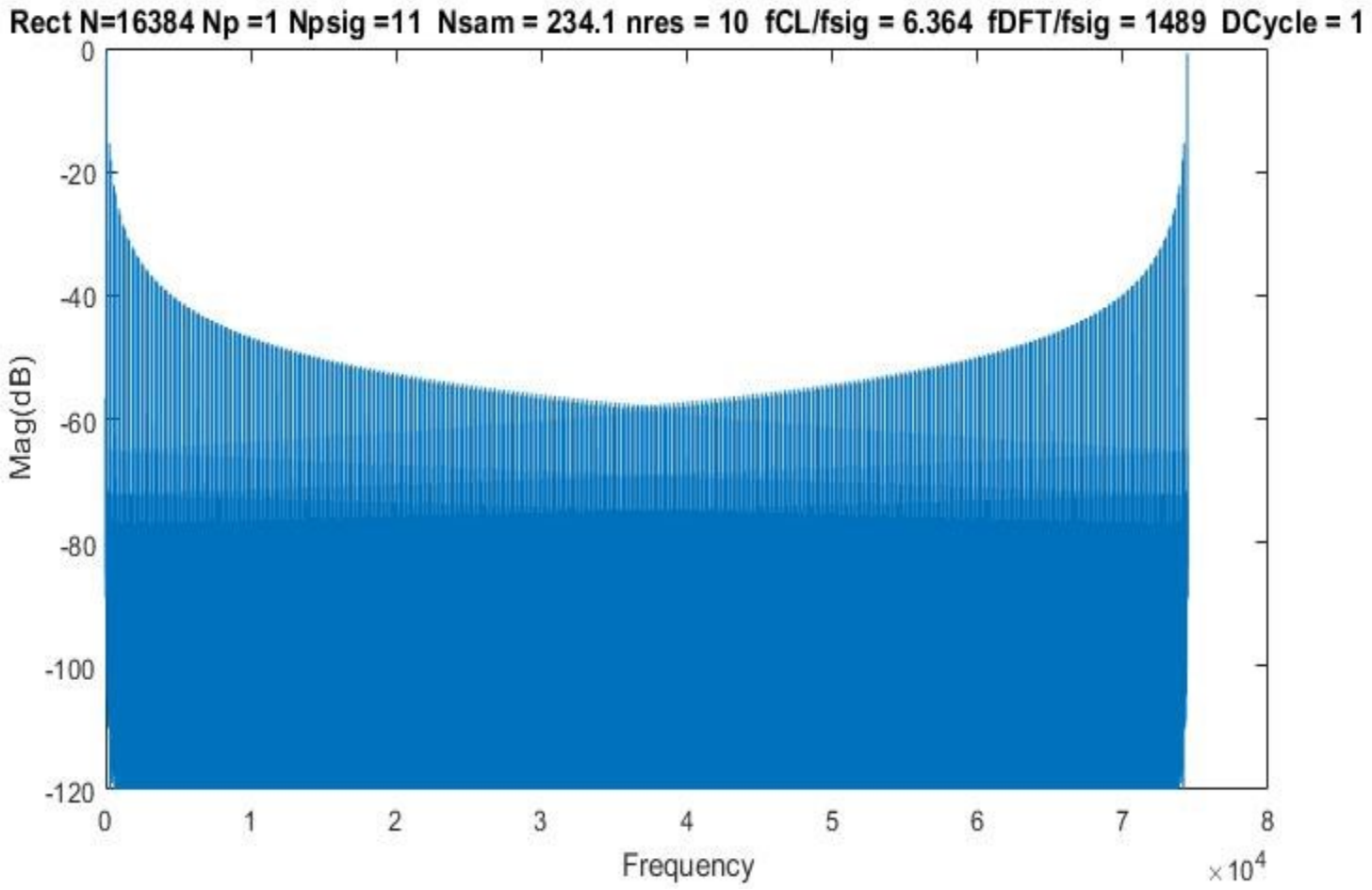


Zero-order Sample and Hold

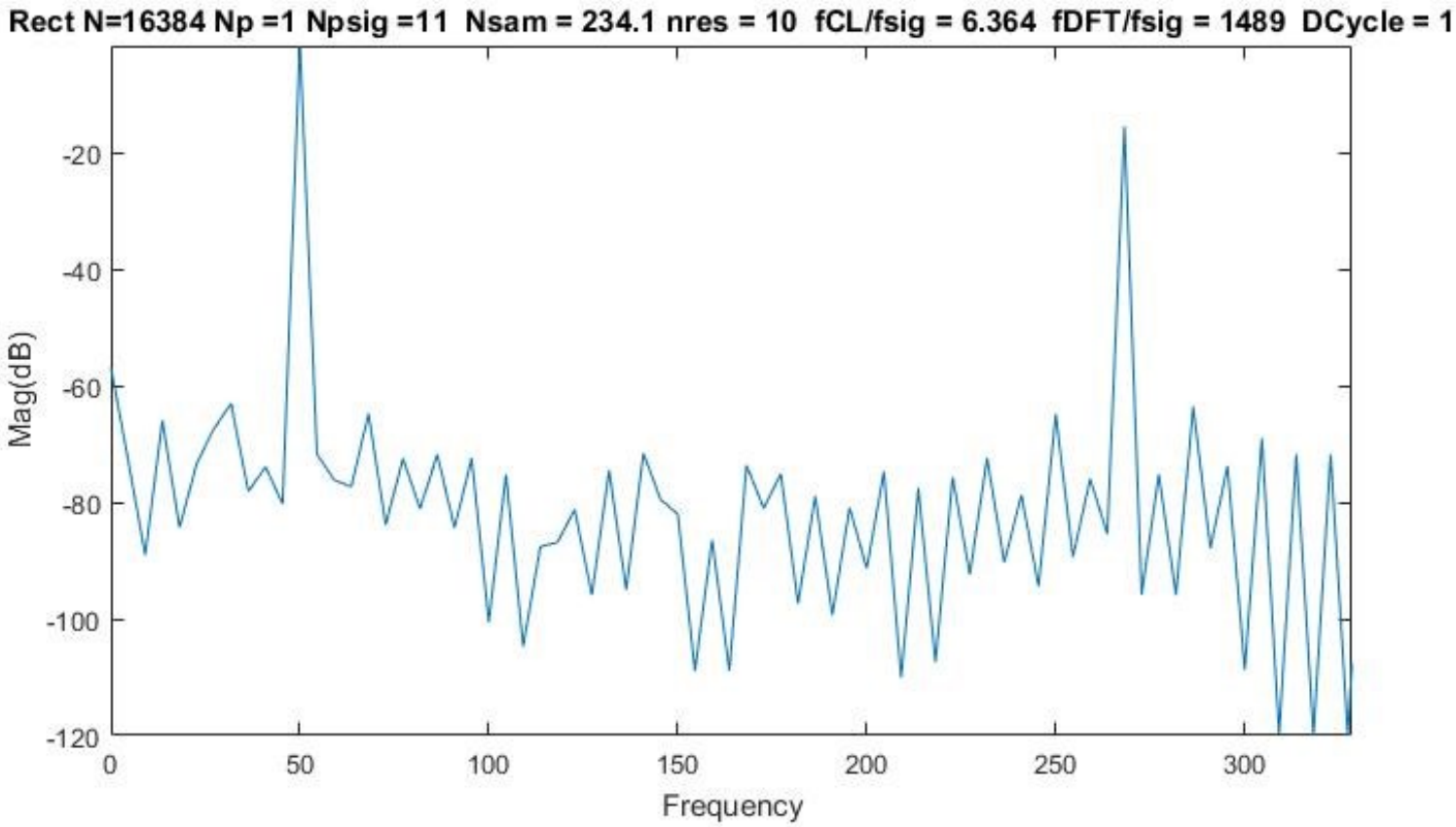
(100% duty cycle)



Zero-order Sample and Hold
(100% duty cycle)



Zero-order Sample and Hold
(100% duty cycle)



Zero-order Sample and Hold
(100% duty cycle)

No spectral distortion components apparent

Magnitude of Fundamental 0.950 2nd Harmonic 0.000
in dB -0.4 -220.0

Res 10 No. points 16384 fsig = 50.00 No.DFT Periods 1.00
No Sig Periods 11.00 fCL/fsig 6.36 Nsamp = 234.06 DutyCycle = 1.0

Rectangular Window
Pyyt =

Columns 1 through 8

-56.7666 -72.6329 -89.0180 -65.9223 -84.2996 -73.2991 -67.3277 -63.0000

Columns 9 through 16

-78.0844 -73.9060 -80.2415 **-0.8009** -71.7226 -76.1473 -77.2781 -64.7624

Columns 17 through 24

-83.8268 -72.4855 -81.0600 -71.7684 -84.3311 -72.4003 **-100.5411** -75.2036

Columns 25 through 32

-104.6890 -87.5996 -86.8260 -81.1797 -95.8796 -74.4617 -94.9546 -71.5626

Columns 33 through 40

-79.4929 -82.0122 -108.8848 -86.4078 -108.8871 -73.6154 -80.9806 -75.0515

Columns 41 through 48

-97.3320 -78.9052 -99.3163 -80.8769 -91.3537 -74.6389 -110.0719 -77.5449

Columns 49 through 56

-107.4100 -75.6450 -92.3523 -72.3248 -90.2704 -78.7130 -94.4099 -64.8687

Columns 57 through 64

-89.3611 -75.9678 -85.3927 -15.3935 -95.8308 -75.1766 -95.9254 -63.5195

Columns 65 through 72

-87.8618 -73.6845 -108.7233 -68.9982 -119.8229 -71.7477 -120.0000 -71.7563

Columns 73 through 80

-119.9494 -68.7360 -109.5559 -73.6204 -89.4074 -63.5185 -97.8093 -74.8683

Columns 81 through 88

-98.2726 -18.1394 -88.4301 -76.0204 -92.7995 -65.1698 -98.4133 -75.7393

Columns 89 through 96

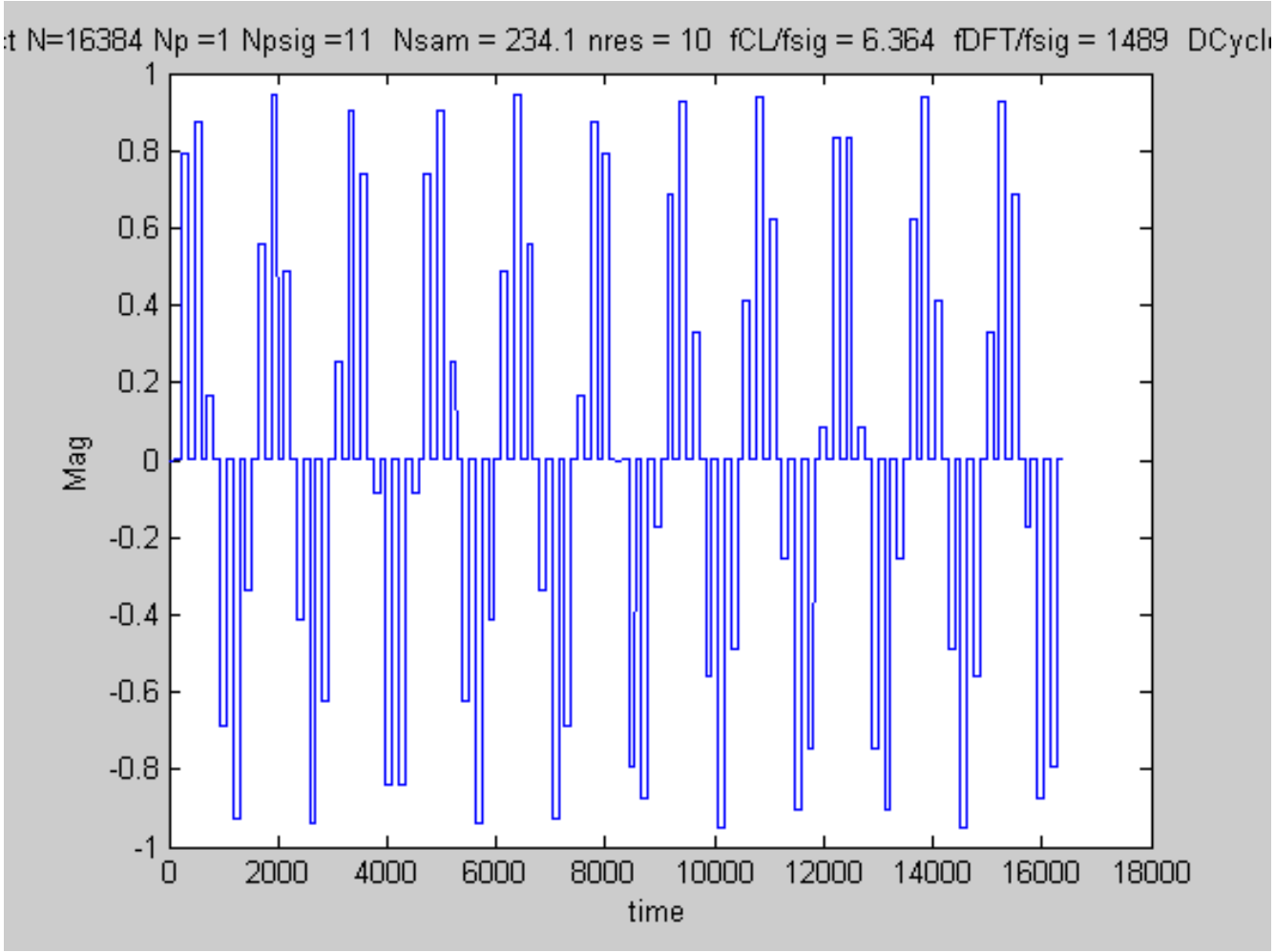
-94.8485 -72.0469 -97.3332 -76.9476 -112.8736 -76.5337 -116.8212 -79.5798

Columns 97 through 104

-98.2141 -81.0207 -106.8397 -76.9870 -105.5319 -79.2621 -89.5668 -79.9400

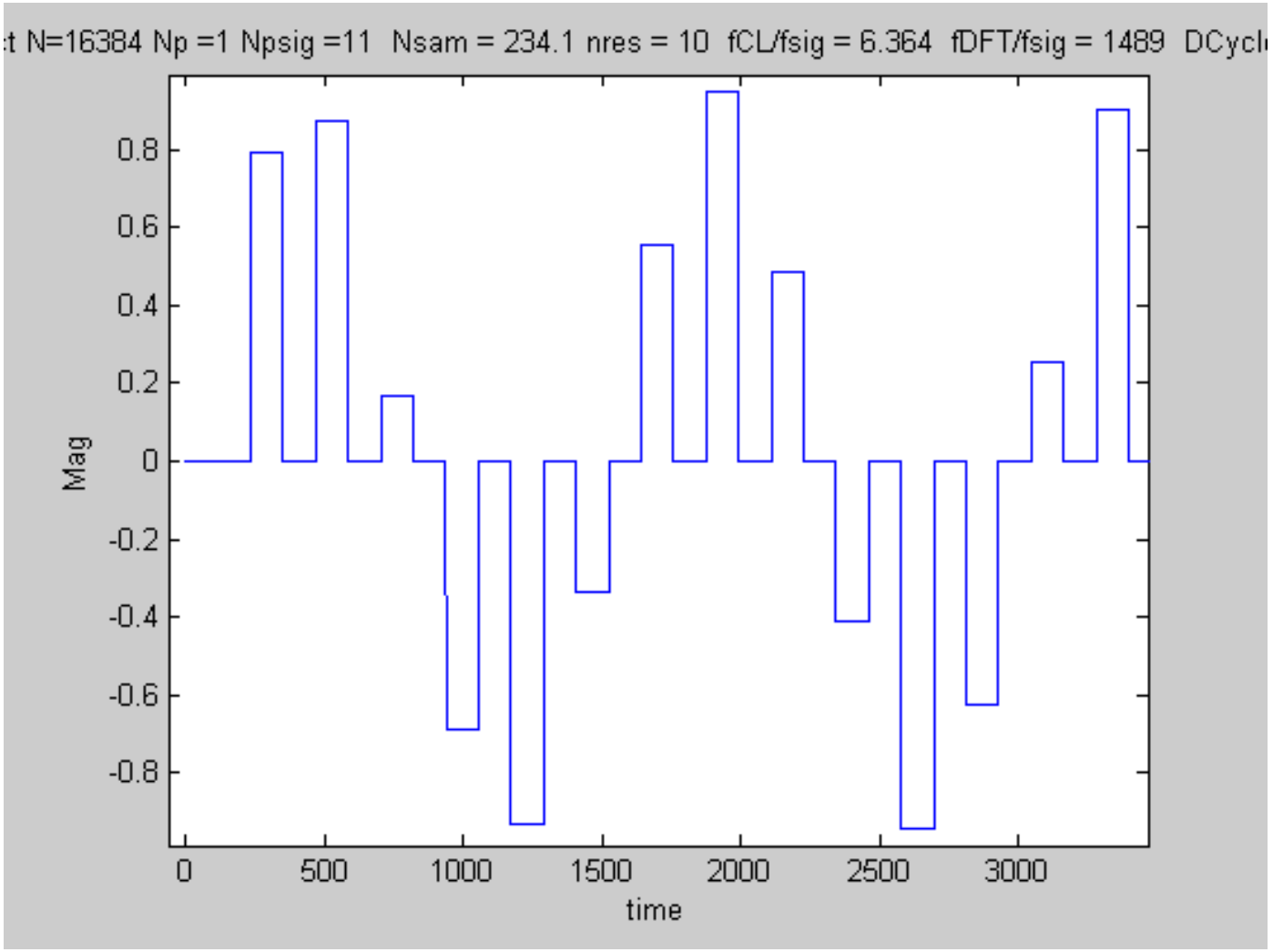
Columns 105 through 110

-118.9287 -86.4077 -117.6606 -76.3449 -90.0484 -82.8245



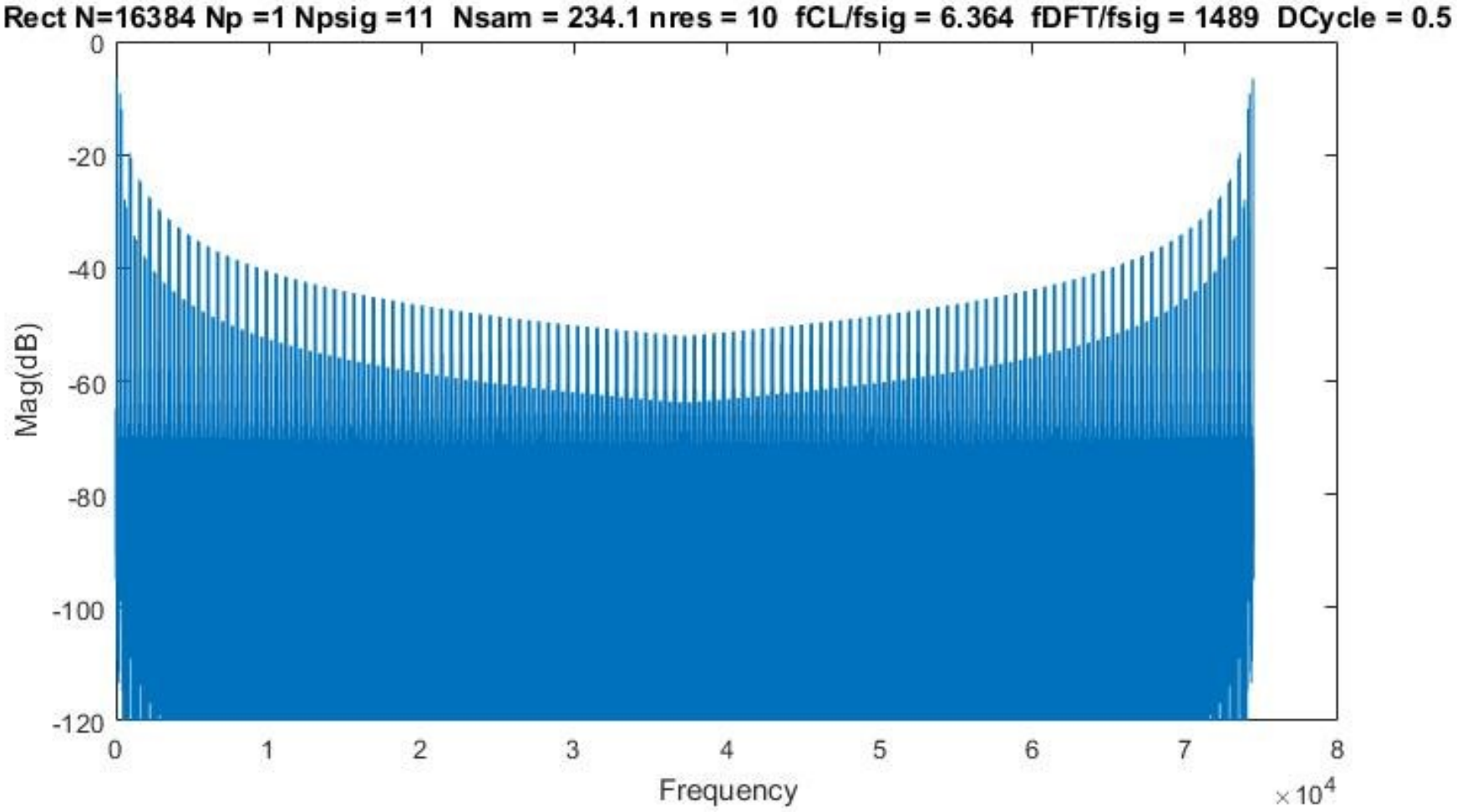
Zero-order Sample and Hold
(50% duty cycle)

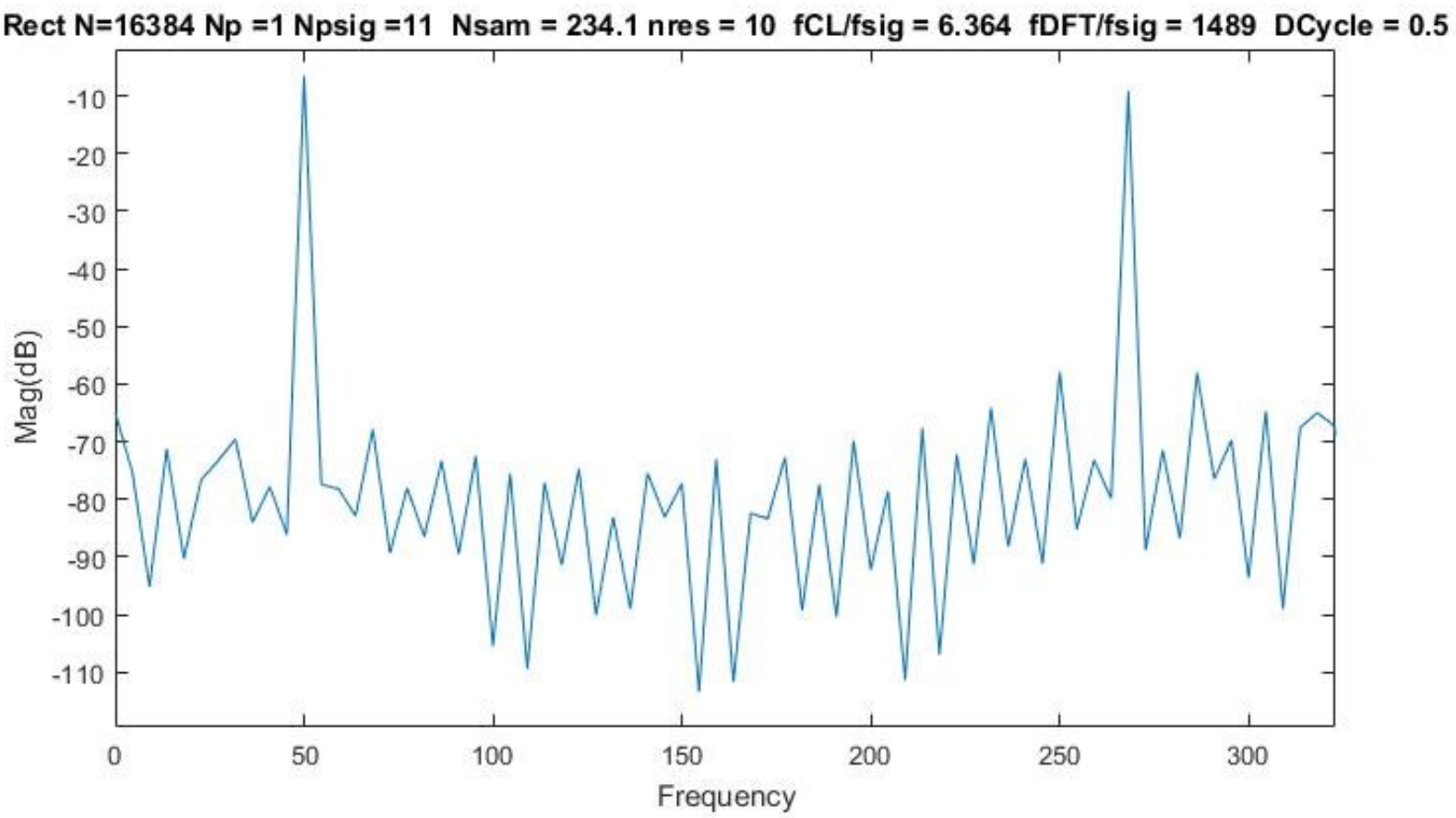
Return to Zero



Zero-order Sample and Hold
(50% duty cycle)

Return to Zero


Rect N=16384 Np =1 Npsig =11 Nsam = 234.1 nres = 10 fCL/fsig = 6.364 fDFT/fsig = 1489 DCycle = 0.5
0
-20
-40
-60
-80
-100
-120
Mag(dB)
0
1
2
3
4
5
6
7
8
Frequency
×10^4


Rect N=16384 Np =1 Npsig =11 Nsam = 234.1 nres = 10 fCL/fsig = 6.364 fDFT/fsig = 1489 DCycle = 0.5
Mag(dB)
-10
-20
-30
-40
-50
-60
-70
-80
-90
-100
-110
0
50
100
150
200
250
300
Frequency

Magnitude of Fundamental 0.950 2nd Harmonic 0.000
in dB -0.4 -220.0
Res 10 No. points 16384 fsig = 50.00 No.DFT Periods 1.00
No Sig Periods 11.0 fCL/fsig 6.36 Nsamp = 234.06 DutyCycle = 0.5

Rectangular Window

Columns 1 through 8

-64.9875 -75.2613 -95.1326 -71.2094 -90.2852 -76.6156 -73.2632 -69.5014

Columns 9 through 16

-83.9643 -77.8162 -86.0866 **-6.5546** -77.4246 -78.1520 -82.8739 -67.8450

Columns 17 through 24

-89.2754 -77.9987 -86.4061 -73.3492 -89.4464 -72.4374 **-105.4623** -75.4661

Columns 25 through 32

-109.3846 -77.1183 -91.3829 -74.6853 -100.0604 -83.0708 -98.8928 -75.4658

Columns 33 through 40

-83.0515 **-77.2072** -113.3805 -73.0081 -111.6998 -82.3913 -83.3412 -72.6823

Columns 41 through 48

-99.2516 -77.3944 -100.3706 -69.8376 **-92.1989** -78.5482 -111.3365 -67.6419

Columns 49 through 56

-106.9480 -72.1848 -91.2497 -64.1067 -88.1852 -72.9575 -91.1348 -57.9429

Columns 57 through 64

-85.1895 -73.1598 -79.8865 -9.1712 -88.8113 -71.4550 -86.7115 -58.0188

Columns 65 through 72

-76.4621 -69.7368 -93.6087 -64.6782 -98.9534 -67.5523 -64.9561 -67.2996

Columns 73 through 80

-98.9315 -63.4010 -94.7247 -69.9035 -77.9584 -58.0242 -89.2150 -71.7656

Columns 81 through 88

-91.2239 -11.9238 -82.9849 -72.9920 -88.6074 -58.0323 -95.6827 -74.9840

Columns 89 through 96

-92.7477 -63.9572 -95.8693 -76.5352 -112.3992 -67.3668 -114.7685 -74.7990

Columns 97 through 104

-99.0492 -69.8650 -109.1443 -75.9390 -107.4431 -70.6650 -92.0134 -75.6831

Columns 105 through 110

-120.0000 -72.9982 -117.8073 -77.0787 -93.6013 -72.8613

DAC Comparisons with Quantization

N	θ	Nsam	n	A_1	A_2	A_3
32K	1	142.5	8	-.596	-56.7	-64.5
128K	1	569.9	8	-.596	-56.7	-64.45
1024	1	6.8	6	-.735	-44.7	-54.1
1024	1	6.8	12	-.594	-80.8	-69.6
1024	1	6.8	24	-.594	-120	-68.5
16K	1	109.2	6	-.729	-44.7	-52.7
16K	1	109.2	12	-.589	-80.8	-90
16K	1	109.2	14	-.589	-120	-92.7
256	1	1.7	18	-.589	-120	-48.2
1024	1	6.8	18	-.595	-120	-68.5
4048	1	27.3	18	-.588	-120	-72.3
16K	1	436.9	18	-.589	-120	-96.5
16K	1	234	10	-.801	-100.5	-82
16K	0.5	234	10	-6.55	-105.4	-77.4

Return to Zero Effects

RTZ reduces signal level

RTZ does not introduce significant distortion

RTZ typically degrades SNR

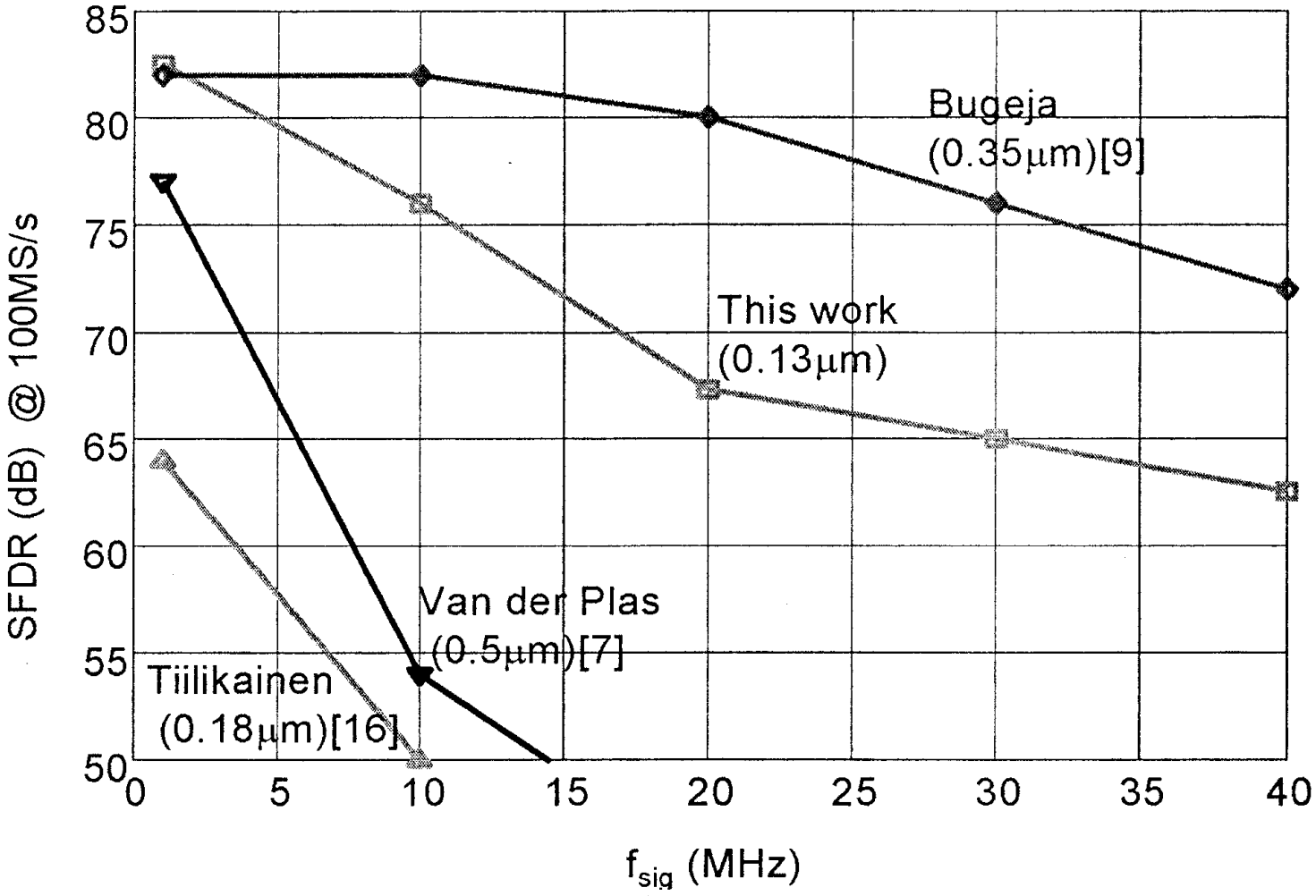
Previous-code dependence in a data converter can introduce significant distortion and this is often significant when operating with high-frequency inputs and high-speed clocks

Return-to Zero can significantly reduce previous-code dependence

RTZ may significantly improve SDR (or SFDR or THD)

Effects of RTZ on SNDR are less apparent since SDR improves but SNR deteriorates but in a good design, the distortion improvements with RTZ may be sufficiently attractive to overcome the loss in SNR

Typical SFDR Plots



RTZ

Zero-Order S/H

From: Y. Cong and R. L. Geiger, "A 1.5-v 14-bit 100-MS/s Self-Calibrated DAC," *IEEE J. of Solid State Circuits*, December 2003, vol. 38, no. 12, pp. 2051-2060.

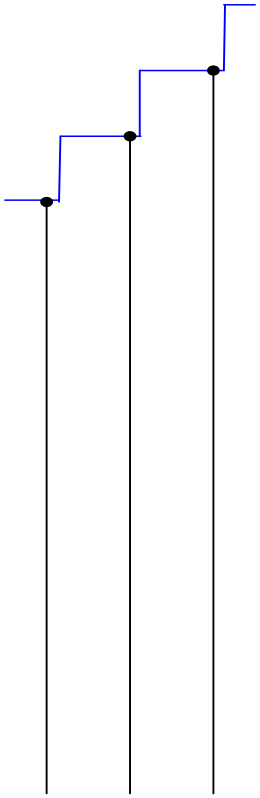
Summary of Duty Cycle Effects

Duty Cycle does not introduce harmonic distortion

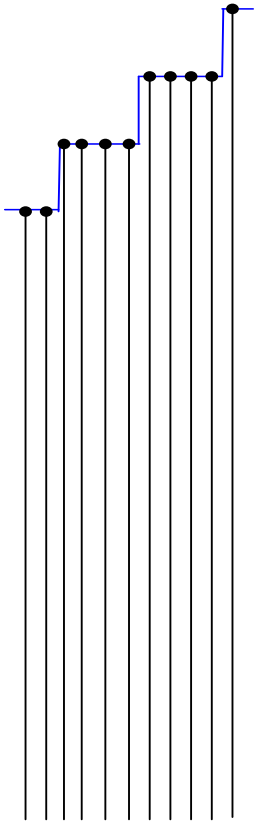
Duty Cycle reduction reduces signal levels thus degrades SNR

Duty Cycle reduction to achieve RTZ can improve SDR and SNDR

Number of Samples/Period



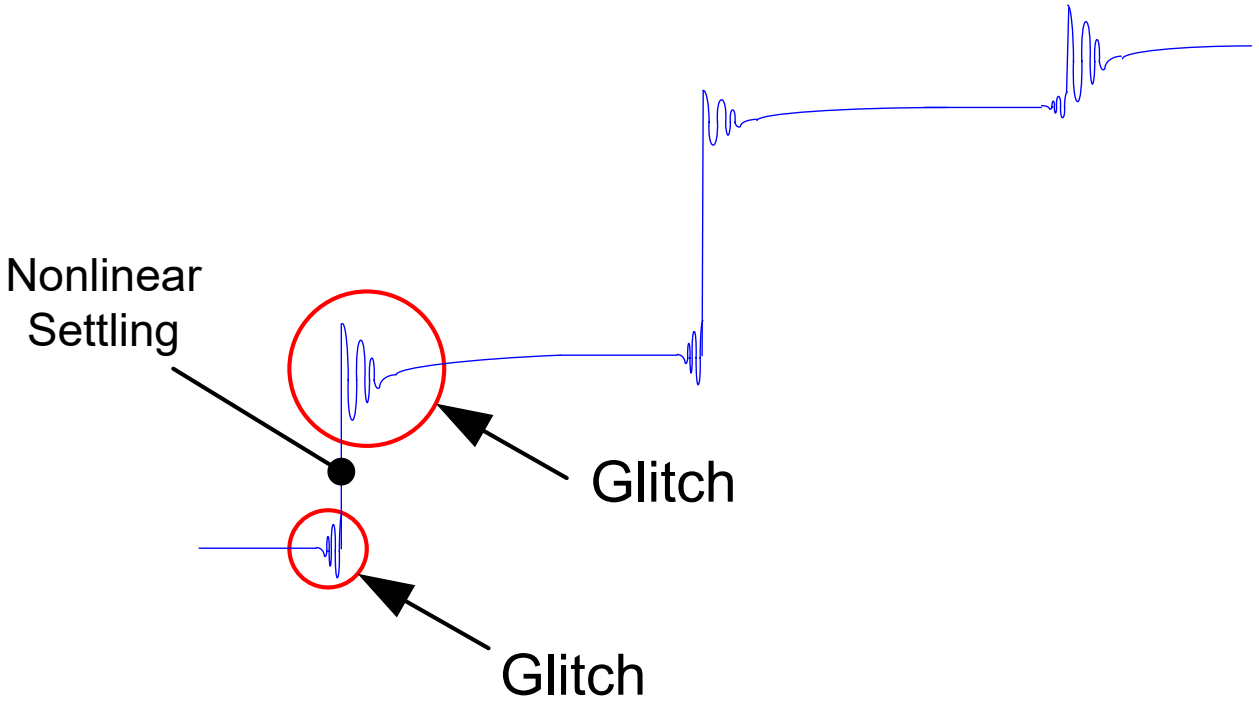
One Sample per Period



Multiple Samples per Period

- Many authors use a data acquisition system and select one sample/period
- Spectrum analyzer will generally measure continuous-time effects
- What is most important in the DAC output is strongly system application dependent

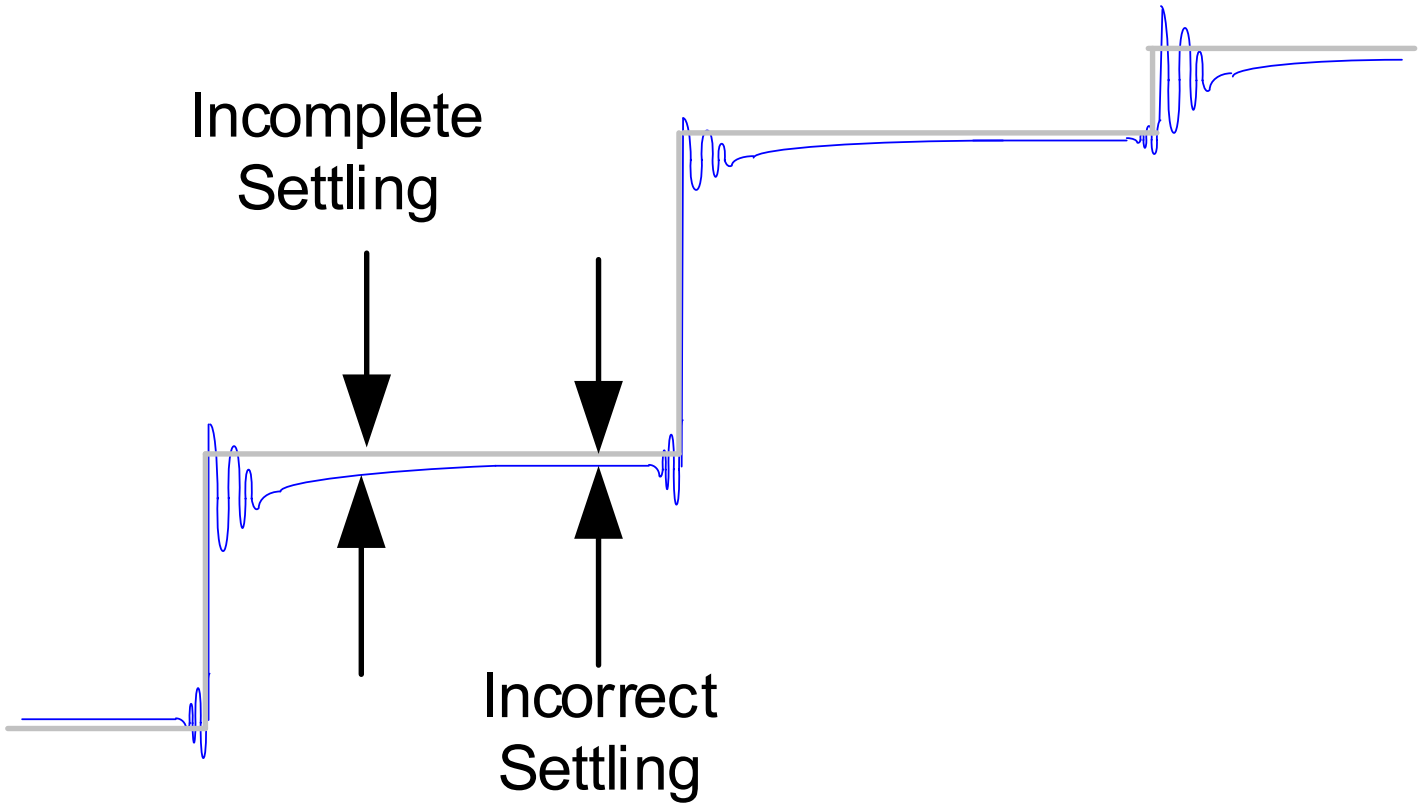
Settling Characteristics of DACs



Typical DAC Response

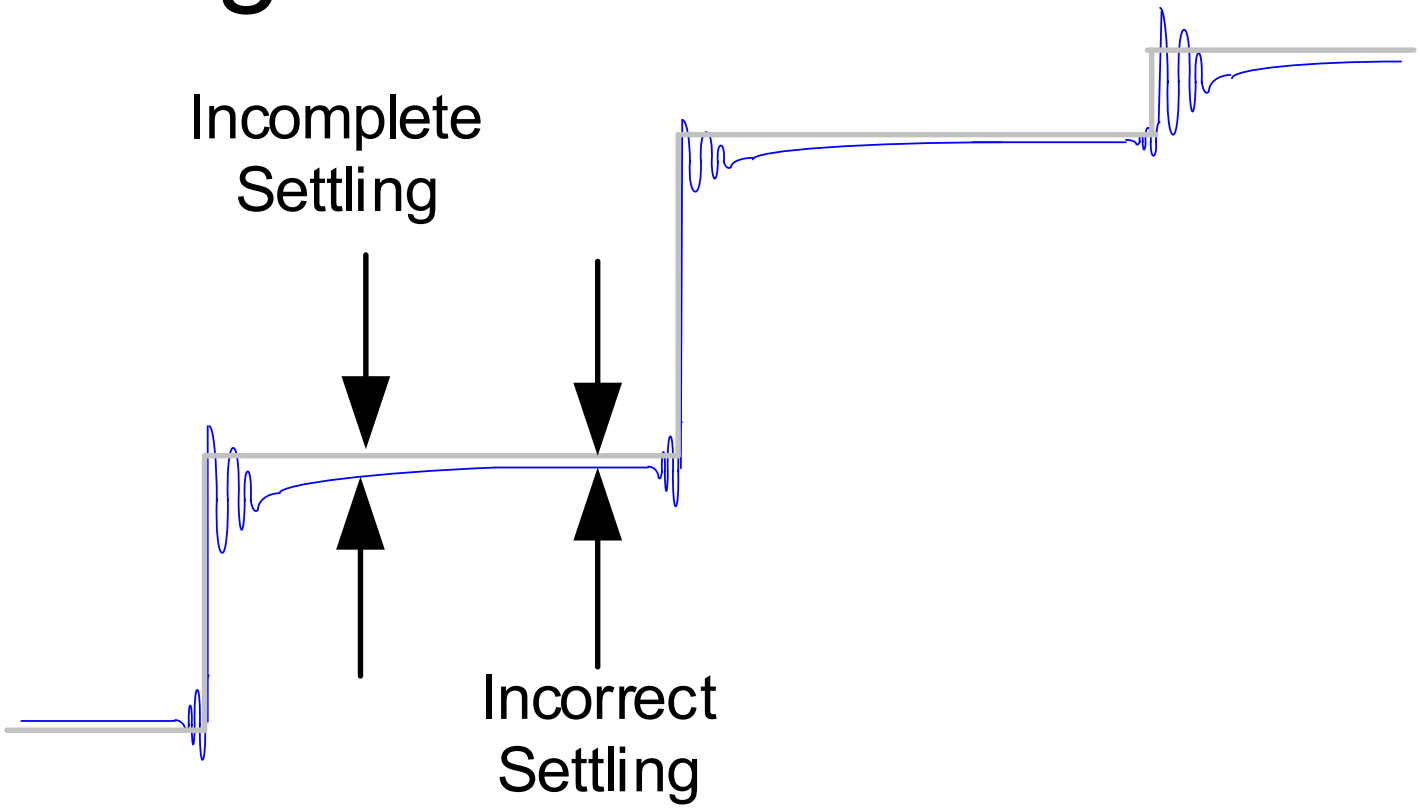
Glitches for even small changes in DAC output for some architectures can be very large (hundreds or even thousands of LSBs)

Settling Characteristics of DACs



Typical DAC Response

Settling Characteristics of DACs

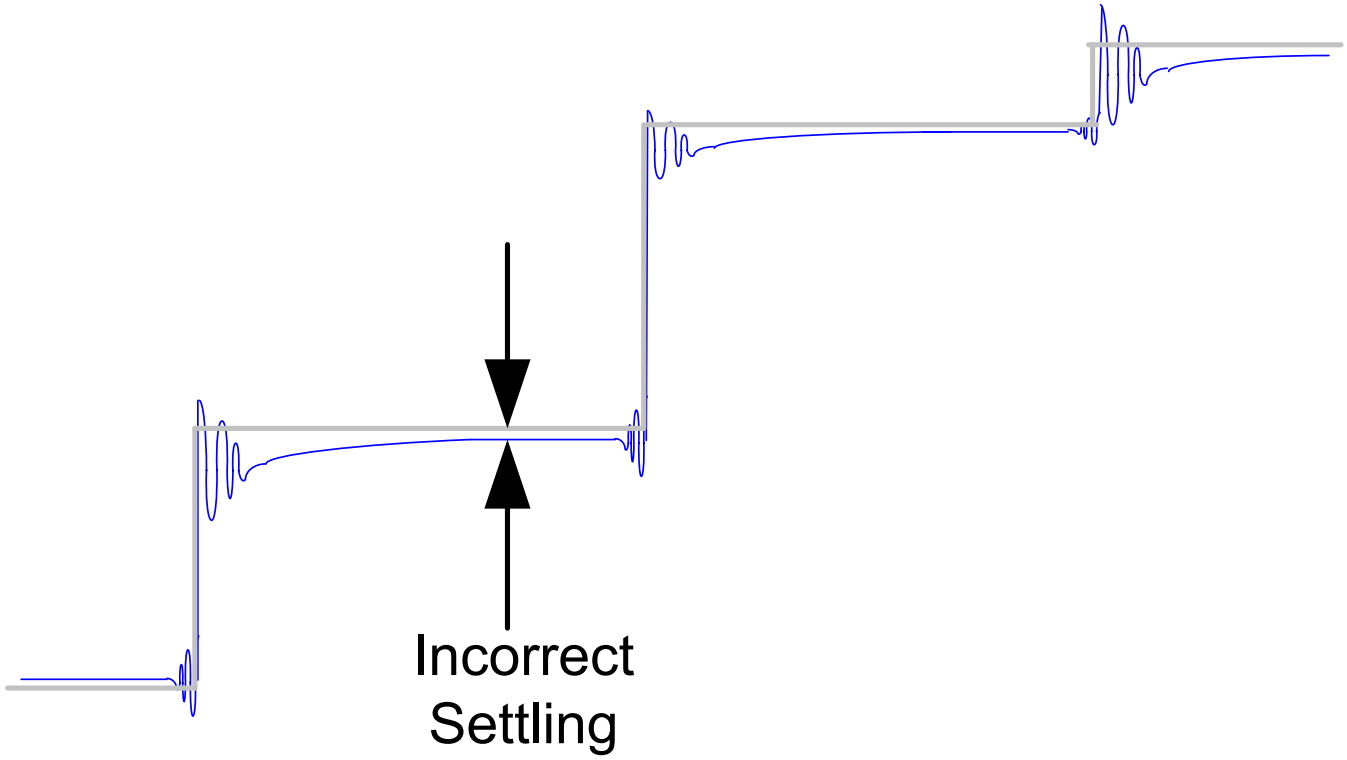


Incomplete Settling: DAC output before steady state achieved

Incorrect Settling: DAC settles to wrong value

Both effects are invariably present when next clock edge occurs in many applications

Settling Characteristics of DACs



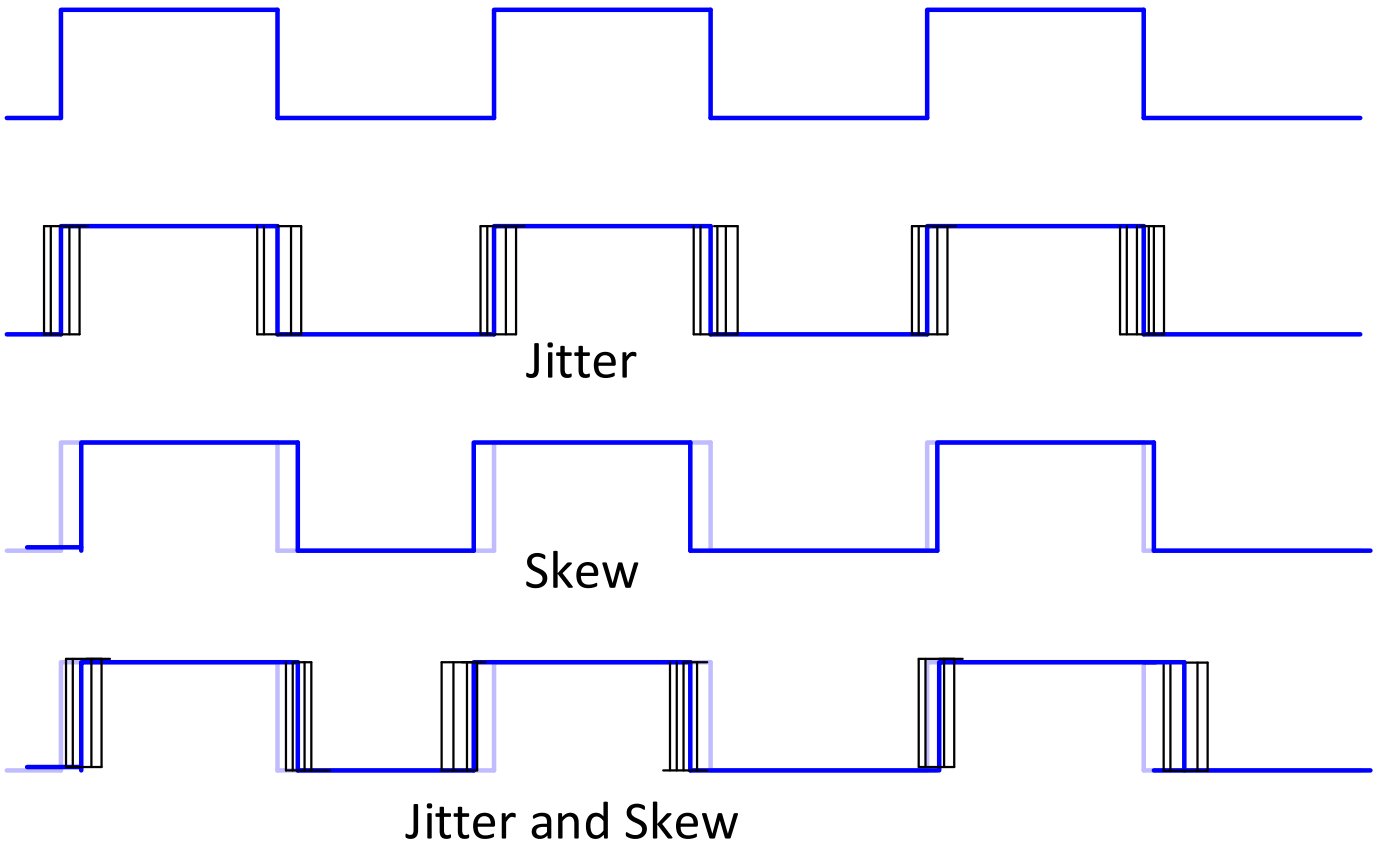
- Settling error can be multiple LSB at Nyquist Rate !!
- Multiple LSB settling error does not cause distortion if settling is linear
- Glitches are a significant contributor to spectral distortion (at high frequencies)

Spectral Characterization of Data Converters

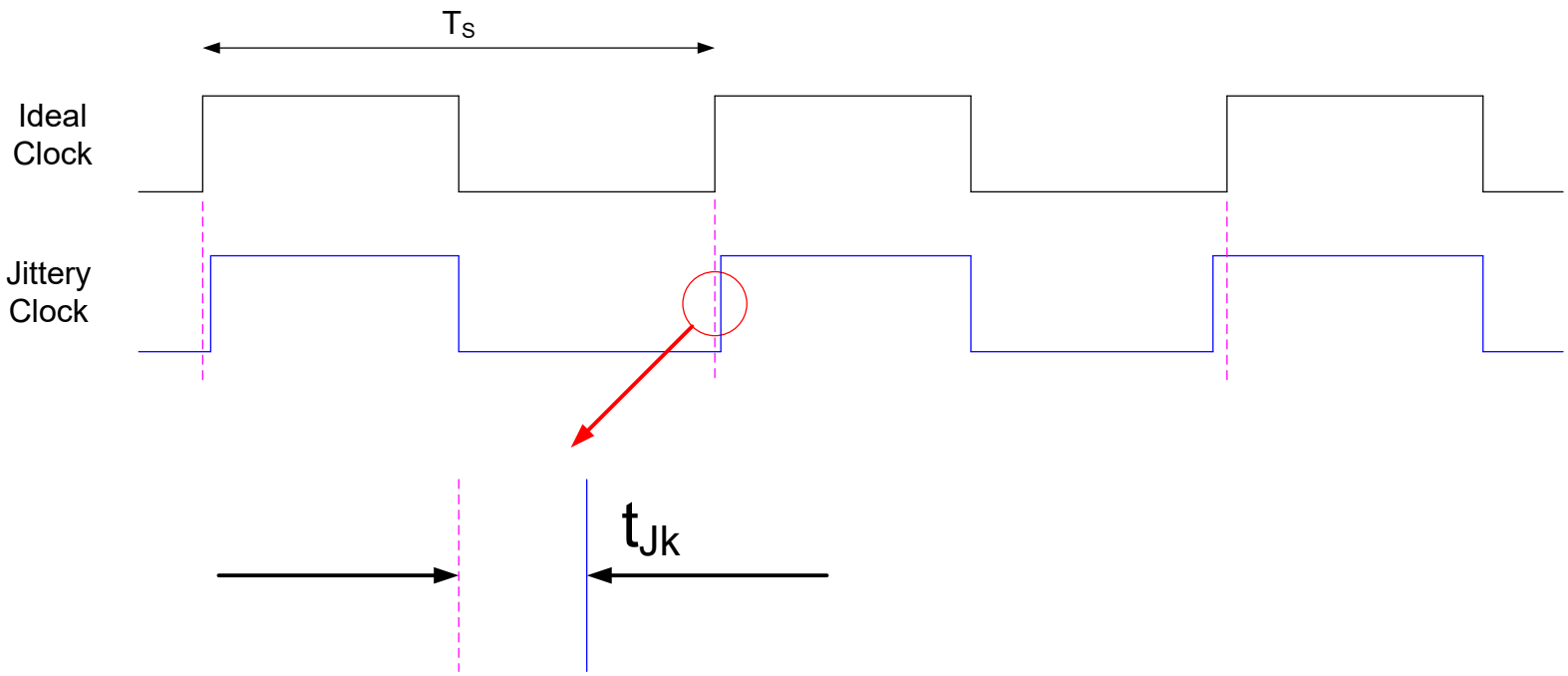
- Distortion Analysis
- Time Quantization Effects
  - of DACs
  - of ADCs
- Amplitude Quantization Effects
  - of DACs
  - of ADCs
- Clock Jitter

Effects of Jitter on Spectral Performance

Jitter and Skew



Model of Jitter



Assume t_{Jk} are uncorrelated uniformly distributed random variables

$$t_{Jk} \propto U\left(-\frac{\theta}{2}T_S, \frac{\theta}{2}T_S\right)$$

Note: there can also be jitter in the ideal clock or there may be no ideal clock so zero crossings may be modeled as a random walk or a sum of a random walk and uniform jitter. Analysis more complicated in these cases.

Analytical Characterization of Clock Jitter

Assume the input can be expressed as

$$v_{IN} = \frac{V_{REF}}{2} + \frac{V_{REF}}{2}\sin(\omega t + \theta)$$

Rather than assuming that the clock has jitter and the input has no jitter, it will be assumed that the clock has no jitter but the input contains the jitter. This should provide the same jitter-based sampling errors. Thus, it will be assumed that the time variable in the input can be expressed as

$$t = t_N + t_R$$

where t_N the nominal time and t_R is the random time (that has been added to the input rather than the clock)

The input can be expanded in a Taylor's series as

$$v_{IN} = v_{IN}\Big|_{t_R=0} + \frac{\partial v_{IN}}{\partial t_R}\Big|_{t_R=0} t_R + \frac{1}{2!}\frac{\partial^2 v_{IN}}{\partial t_R^2}\Big|_{t_R=0} t_R^2 + \ldots.$$

Truncating after first-order terms we have

$$v_{IN} \cong v_{IN}\Big|_{t_R=0} + \frac{\partial v_{IN}}{\partial t_R}\Big|_{t_R=0} t_R$$

Analytical Characterization of Clock Jitter

$$v_{IN} \cong v_{IN}\Big|_{t_R=0} + \frac{\partial v_{IN}}{\partial t_R}\Big|_{t_R=0} t_R$$

It now follows from the expression from the input that

$$\frac{\partial v_{IN}}{\partial t_R}\Big|_{t_R=0} = \frac{V_{REF}}{2}\omega\cos(\omega t_N + \theta)$$

Thus

$$v_{IN} \cong \frac{V_{REF}}{2} + \frac{V_{REF}}{2}\sin(\omega t_N + \theta) + \frac{V_{REF}}{2}\omega\cos(\omega(t_N) + \theta)t_R$$

The signal and noise jitter components can be identified as

$$v_{IN\_Sig} \cong \frac{V_{REF}}{2} + \frac{V_{REF}}{2}\sin(\omega t_N + \theta)$$

$$v_{IN\_jitter} \cong \frac{V_{REF}}{2}\omega\cos(\omega(t_N) + \theta)t_R$$

Analytical Characterization of Clock Jitter

$$v_{IN\_Sig} \cong \frac{V_{REF}}{2} + \frac{V_{REF}}{2}\sin(\omega t_N + \theta)$$

$$v_{IN\_jitter} \cong \frac{V_{REF}}{2}\omega\cos(\omega(t_N) + \theta)t_R$$

Will now obtain the SNR_{Jitter}

Observe the jitter noise can be expressed as

$$v_{IN\_jitter} \cong \left[\frac{V_{REF}}{2}\omega\cos(\omega(t_N) + \theta)\right] \bullet t_R$$

Consider the following theorem:

Theorem: If $X_1(t)$ is a zero-mean random process and $X_2(t)$ is a periodic deterministic function where the RMS value of X_1 is X_{1RMS} and the RMS value of X_2 is X_{2RMS}, then the RMS value of the product is given by the expression $X_{RMS}=X_{1RMS}X_{2RMS}$

Analytical Characterization of Clock Jitter

$$v_{\text{IN\_jitterRMS}} \cong \left[\frac{V_{REF}}{2}\omega\cos\left(\omega(t_N)+\theta\right)\right]_{RMS} \bullet t_R\big|_{RMS}$$

$$\left[\frac{V_{REF}}{2}\omega\cos\left(\omega(t_N)+\theta\right)\right]_{RMS} = \left[\frac{V_{REF}}{2}\frac{\omega}{\sqrt{2}}\right]$$

Recall it has been assumed that at the zero crossings of the sampling clock

$$t_R \propto U\left(-\frac{\theta}{2}T_S, \frac{\theta}{2}T_S\right) \qquad \mu_{t_R} = 0 \qquad \sigma_{t_R} = \frac{\theta T_S}{\sqrt{12}}$$

Recall another theorem

Theorem: If n(t) is a random process and $\langle n(kT_S)\rangle$ is a sequence of samples of n(t) then for large T/T_S,

$$V_{RMS} = \sqrt{\frac{1}{T}\int_{t_1}^{t_1+T} n^2(t)\,dt} = \sqrt{\sigma^2_{n(kT_S)} + \mu^2_{n(kT_S)}}$$

Thus the RMS value of the jitter time sequence obtained by sampling the jitter at multiples of the nominal sampling period T can be expressed as

$$t_R\big|_{RMS} = \sigma_{t_R} = \frac{\theta T_S}{\sqrt{12}}$$

Analytical Characterization of Clock Jitter

$$v_{\text{IN\_jitterRMS}} \cong \left[\frac{V_{REF}}{2}\omega\cos\left(\omega\left(t_N\right)+\theta\right)\right]\Bigg|_{RMS} \bullet t_R\big|_{RMS}$$

We thus have

$$v_{\text{IN\_jitterRMS}} \cong \left[\frac{\frac{V_{REF}}{2}\omega}{\sqrt{2}}\right] \bullet \sigma_{t_R}$$

For full-signal input, the RMS value is given by

$$v_{\text{IN\_SigRMS}} \cong \frac{V_{REF}}{2\sqrt{2}}$$

It thus follows that the SNR is given by

$$SNR_{Jitter} = \frac{\frac{V_{REF}}{2\sqrt{2}}}{\left[\frac{\frac{V_{REF}}{2}\omega}{\sqrt{2}}\right] \bullet \sigma_{t_R}} = \frac{1}{\omega\sigma_{t_R}}$$

Analytical Characterization of Clock Jitter

$$SNR_{Jitter} = \frac{1}{\omega \sigma_{t_R}}$$

Or in dB we thus have

$$SNR_{Jitter\_dB} = -20\log\left(2\pi f \sigma_{t_R}\right)$$

$$SNR_{Jitter\_dB} = -15.96 - 20\log\left(f \sigma_{t_R}\right)$$

For small f or σ_{tR} the right-most term is large and positive

This can be compared to the quantization noise

$$SNR_{Quant\_dB} = 6.02n + 1.76$$

As the f σ_{tR} product gets large, the jitter will dramatically degrade performance

Combined Quantization and Jitter Noise

$$v_{\text{noiseRMS}} = \sqrt{v_{QuantRMS}^2 + v_{\text{IN\_jitterRMS}}^2}$$

Recall

$$v_{Quant\text{RMS}} = \frac{V_{LSB}}{\sqrt{12}} = \frac{V_{REF}}{2^n\sqrt{12}}$$

$$v_{Sig\text{RMS}} = \frac{V_{REF}}{2\sqrt{2}}$$

Thus

$$SNR_{Jitter-Quant} = \frac{\frac{V_{REF}}{2\sqrt{2}}}{\sqrt{\left[\frac{\frac{V_{REF}}{2}\omega}{\sqrt{2}}\right]^2 \sigma_{t_R}^2 + \frac{V_{REF}^2}{2^{2n} \bullet 12}}} = \frac{1}{\sqrt{\omega^2\sigma_{t_R}^2 + \frac{8}{3 \bullet 2^{2n+2}}}}$$

Alternately

$$SNR_{Jitter-Quant} = \frac{1}{\sqrt{\frac{1}{SNR_{Jitter}^2} + \frac{1}{SNR_{Quant}^2}}}$$

$$SNR_{Jitter-QuantdB} = -10\log\left(\frac{1}{SNR_{Jitter}^2} + \frac{1}{SNR_{Quant}^2}\right)$$

Combined Quantization and Jitter Noise

$$SNR_{Jitter-Quant} = \frac{1}{\sqrt{\omega^2 \sigma_{t_R}^2 + \frac{8}{3 \bullet 2^{2n+2}}}}$$

Crossover Frequency

$$f = \frac{1}{\pi \sigma_{t_R}} \sqrt{\frac{8}{3}} \frac{1}{2^{n+2}} = \frac{0.13}{\sigma_{t_R} 2^n}$$

Model of Jitter

Assume t_{Jk} are uncorrelated uniformly distributed random variables

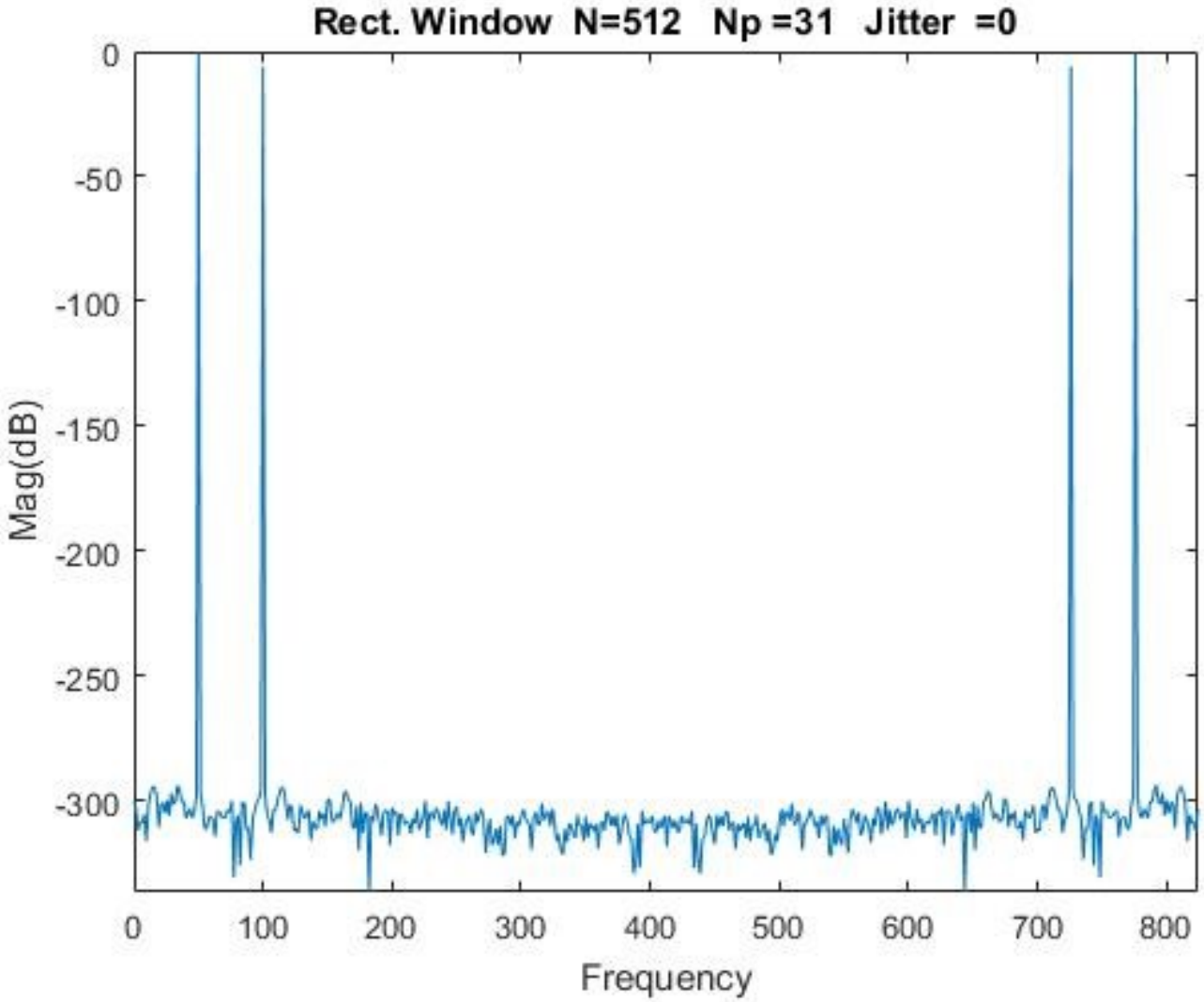
$$t_{Jk} \propto U\left(-\frac{\theta}{2}T_S,\ \frac{\theta}{2}T_S\right)$$

Consider θ=.01, .001, .0001, .00001

Observe: If T_S is a 100MHz clock, then T_S=10nsec and θ=.0001 corresponds to 1psec (±0.5psec) of symmetric jitter

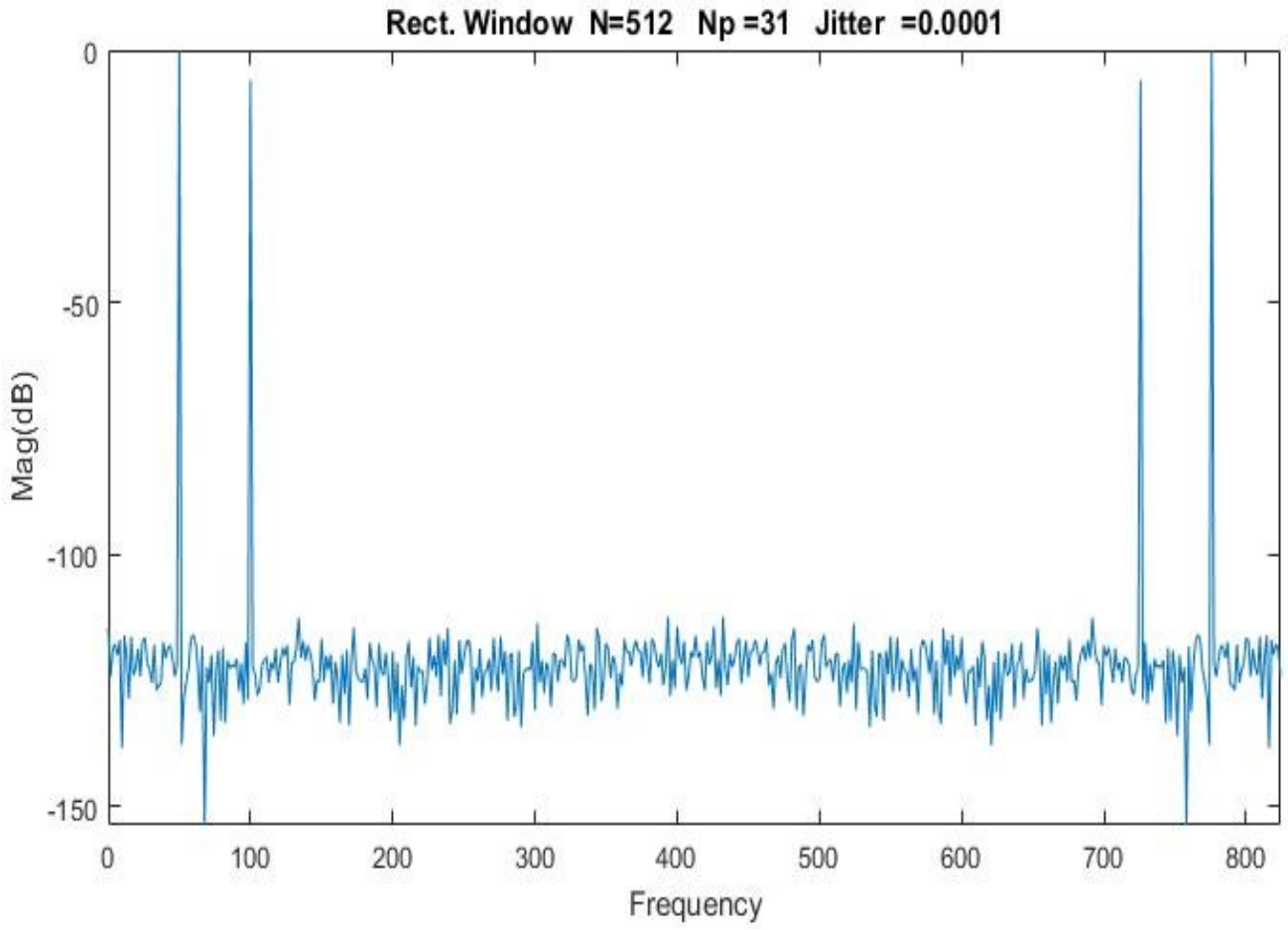
Effects of jitter on spectral performance

$$V_{IN} = \sin(\omega t) + 0.5\sin(2\omega t) \qquad \omega = 2\pi f_{sig} \qquad f_{sig} = 50\text{Hz}$$



Effects of jitter on spectral performance

$$V_{IN} = \sin(\omega t) + 0.5\sin(2\omega t) \qquad \omega = 2\pi f_{sig} \qquad f_{sig} = 50\text{Hz}$$



Effects of jitter on spectral performance

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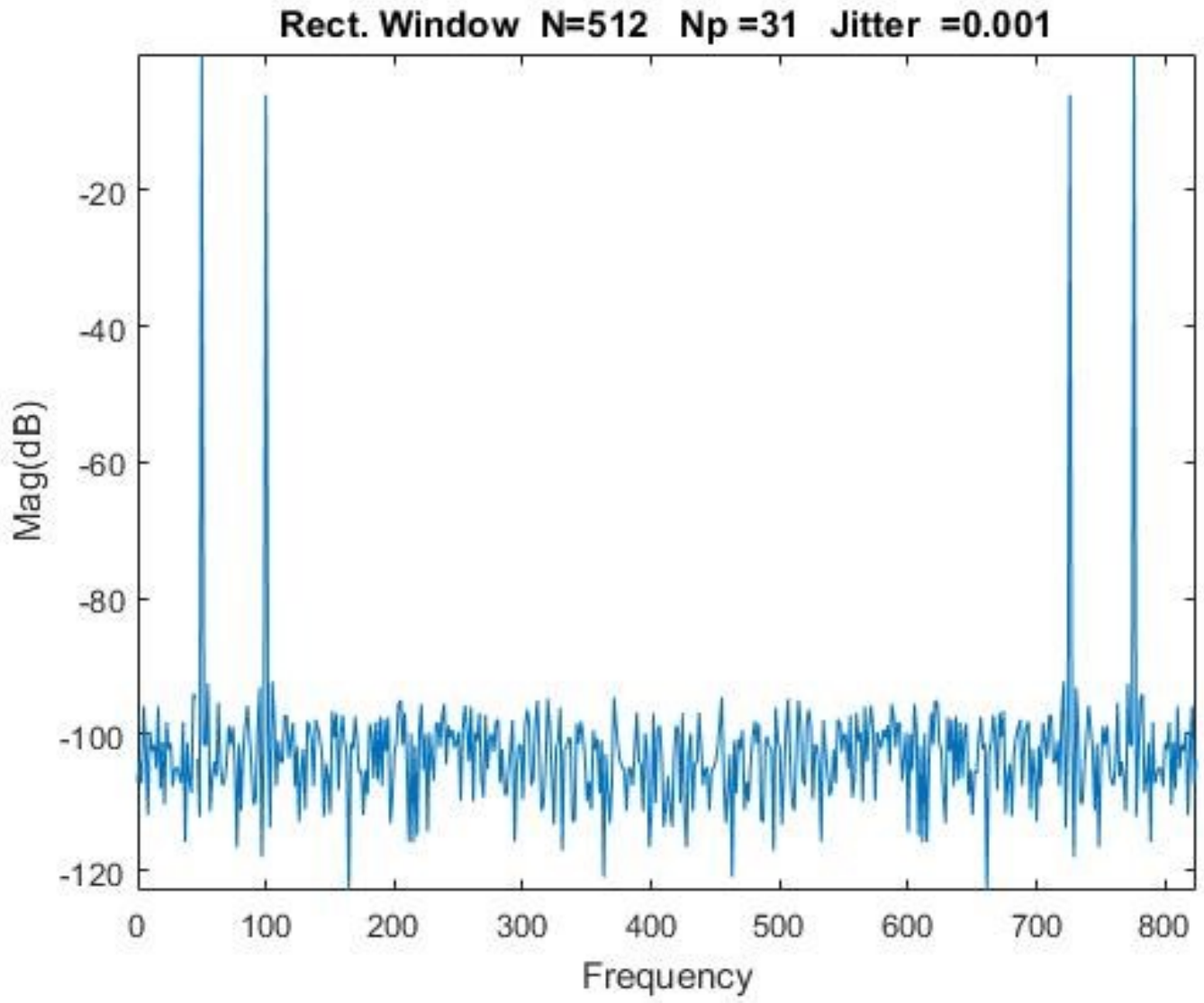

Effects of jitter on spectral performance

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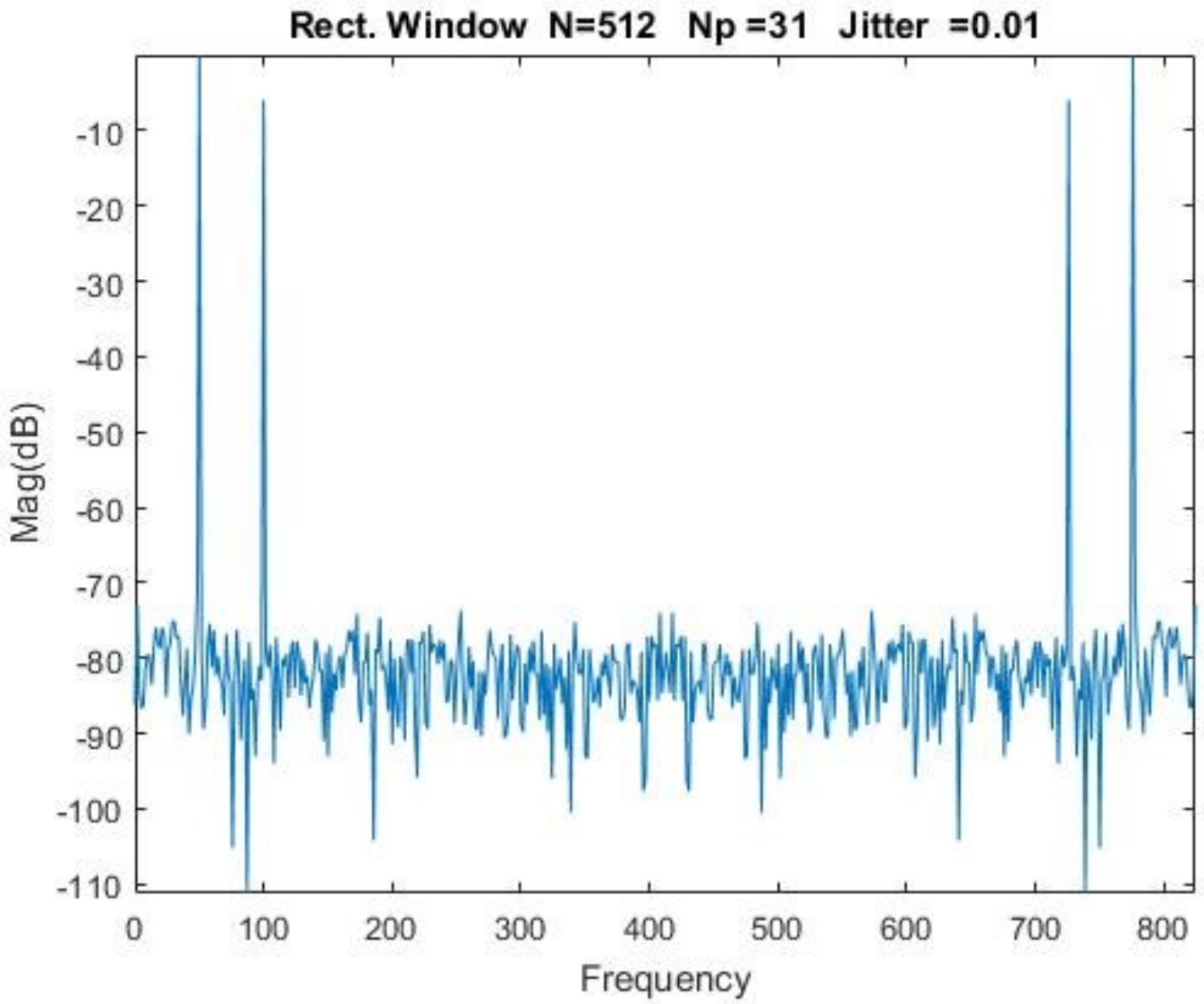


Summary of Jitter Effects

Jitter (as considered here) does not introduce harmonic distortion

Jitter does increase the noise floor

Jitter vs Clock Skew

- Jitter and Clock skew may appear to be closely related but have dramatically different effects
- Clock Skew is a systematic perturbation of the clock signal
- Clock Skew may be a random variable at the design stage but each fabricated device will have a specific clock skew
- Clock edge variations from ideal will be the sum of those variations due to random noise and those due to clock skew
- In contrast to jitter which does not introduce harmonic distortion, clock skew can introduce spectral components, specifically harmonic components and spectral spreading around the spectral components of the fundamental and harmonics

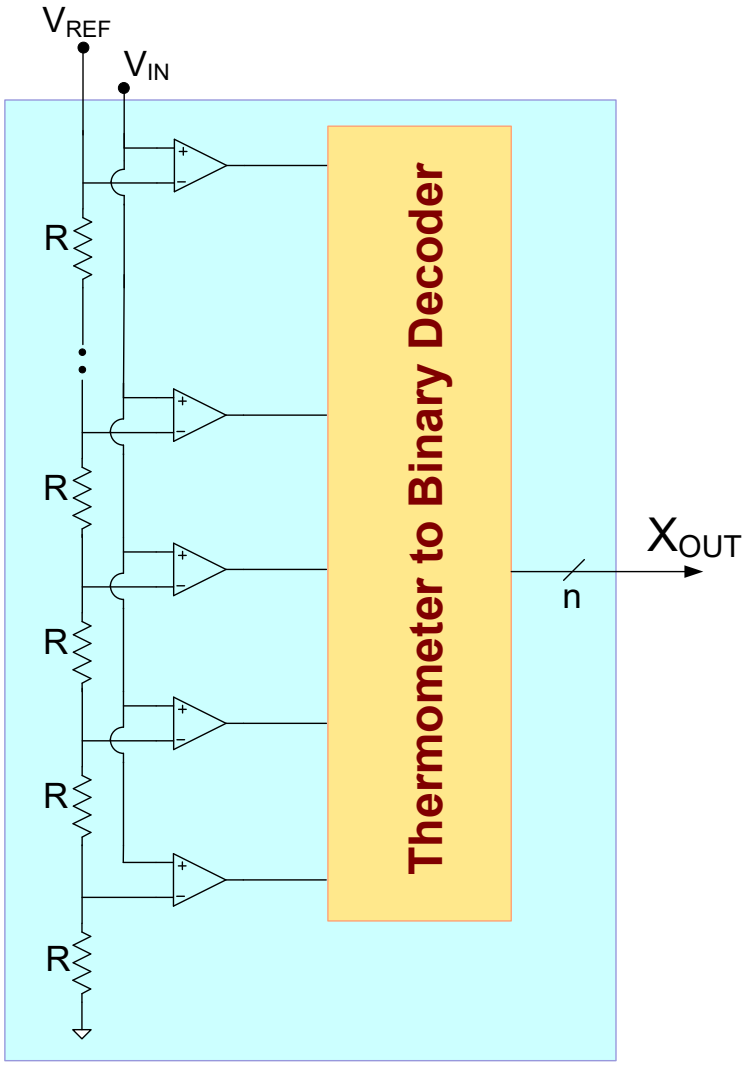
Statistical Characterization of Electronic Components and Circuits

Recall: Almost all data converter structures work perfectly if components are ideal

Major challenges in data converter design

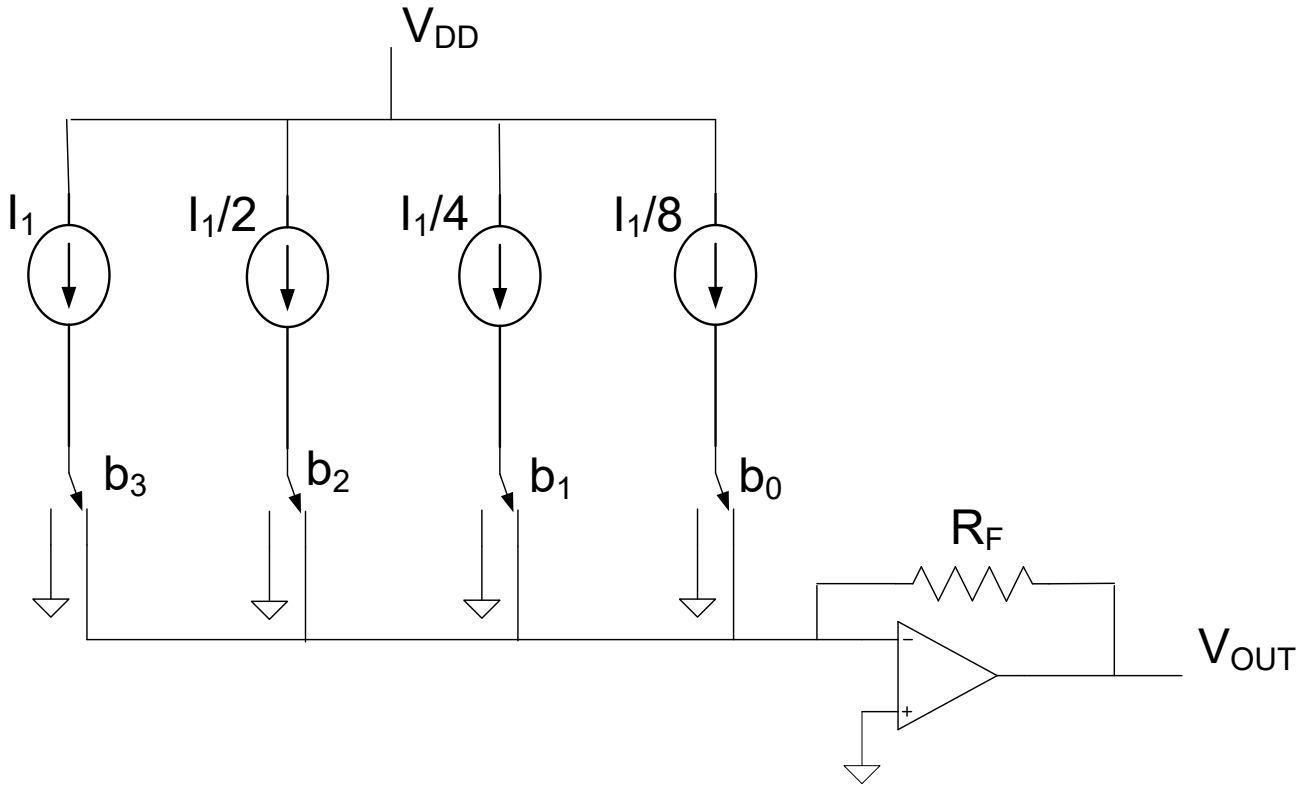
- Parasitic Resistances and Capacitances
- Nonlinearity in components
- Statistical variation in components and circuits
- Model uncertainties
- Power supply variability

Consider a flash ADC



- Resistor values and offset voltages of Comparators are all random variables at design level
- Variations of these RVs affect the break point and thus the yield

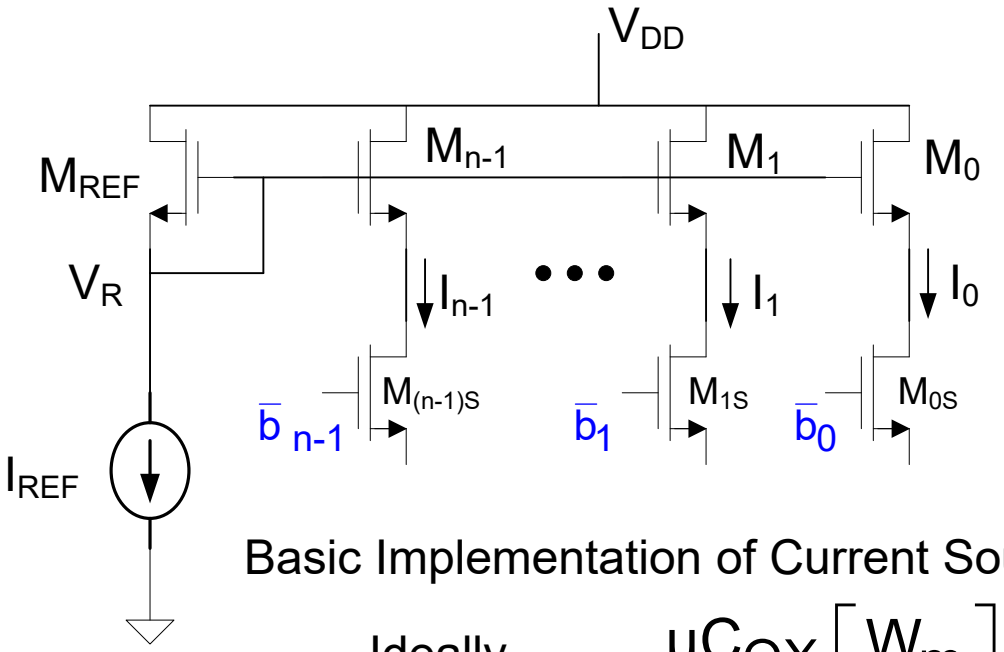
Consider Current-Steering DAC

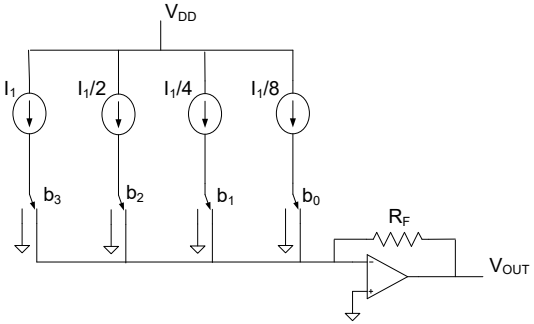


Ideally

$$V_{OUT} = -I_1 \bullet R_F \sum_{i=0}^{n-1} \frac{b_i}{2^{n-i}}$$

Consider Current-Steering DAC





Basic Implementation of Current Sources

Ideally $$I_m = \frac{\mu C_{OX}}{2}\left[\frac{W_m}{L_m}\right]\left(V_R - V_{Tp}\right)^2$$

$L_m = L_0$

$W_m = 2^{m-1} W_0$

Actually $$I_m \cong \frac{\mu_k C_{OXk}}{2}\left[\frac{W_{m_k}}{L_{m_k}}\right]\left(V_R - V_{Tpk}\right)^2$$

I_m is a random variables and is a function of the model parameters μ_k, C_{OXk}, W_{mk}, L_{mk}, and V_{Tpk}

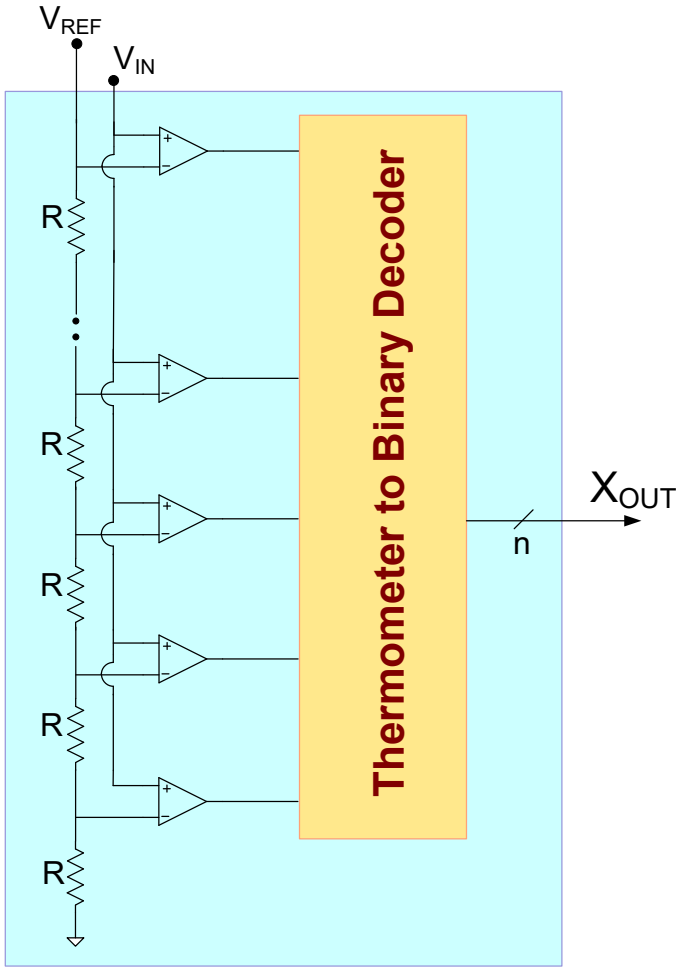
μ_k, C_{OXk}, W_{mk}, L_{mk}, and V_{Tpk} are all random variables

Recall from previous lecture

How important is statistical analysis?

Example: 7-bit FLASH ADC with R-string DAC

Assume R-string is ideal, V_{REF}=1V and V_{OS} for each comparator must be at most +/- ½ LSB



Case 1

Standard deviation is 5mV

P_{COMP} = 0.565

$Y_{ADC}=3.2 \bullet 10^{-32}$

Case 2

Standard deviation is 1mV

P_{COMP} = 0.999904

$Y_{ADC}=0.988$

Statistics play a key role in the performance and consequently yield of a data converter

Statistical Analysis Strategy

Will first focus on statistical characterization of resistors, then extend to capacitors and transistors

Every resistor R can be expressed as

$$R=R_N+R_{RP}+R_{RW}+R_{RD}+R_{RGRAD}+R_{RL}$$

where R_N is the nominal value of the resistor and the remaining terms are all random variables

R_{RP}: Random process variations
R_{RW}: Random wafer variations
R_{RD}: Random die variations
R_{RGRAD}: Random gradient variations
R_{RL}: Local Random Variations

- Data Converters (ADCs and DACs) are ratiometric devices and performance often dominated by ratiometric device characteristics (e.g. matching)
- Many other AMS functions are dependent upon dimensioned parameters and often not dependent upon matching characteristics

Statistical Analysis Strategy

$$R=R_N+R_{RP}+R_{RW}+R_{RD}+R_{RGRAD}+R_{RL}$$

R_{RP}: Random process variations
R_{RW}: Random wafer variations
R_{RD}: Random die variations
R_{RGRAD}: Random gradient variations
R_{RL}: Local Random Variations

$$\sigma_{RP} >> \sigma_{RW} >> \sigma_{RD}$$

- All variables globally uncorrelated
- For good common-centroid layouts gradient effects can be neglected
- Local random variations often much smaller than R_{RP}, R_{RW}, and R_{RD} though not necessarily
- Area dominantly determines σ_{RL}, but area has little effect on the other variables
- At the resistor-level on a die, R_{RP}, R_{RW} and R_{RD} highly correlated thus cause no mismatch
- Major challenge in data converter design is managing R_{RL} effects
- All zero mean and approximately Gaussian (truncated)
- For dimensioned performance characteristics (e.g. band edge of filter), R_{RP}, R_{RW} and R_{RD} are dominant and R_{RGRAD} and R_{RL} typically secondary

For notational convenience, assume $R=R_N+R_R$

R_N includes R_{RP}, R_{RW} and R_{RD}, R_{GRAD} neglected, $R_R=R_{RL}$

Stay Safe and Stay Healthy !

End of Lecture 8